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Optimizing Schottky barrier diodes: the role of PVC and PVC: molybdenum interlayers in electrophysical properties

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ABSTRACT

In this research, the n-Si wafer is used to generate Au/n-Si (C_0), Au/PVC/n-Si (C_1), and Au/PVC: Molybdenum (Mo)/n-Si (C_2) structures to examine the effects of PVC and PVC:Mo interlayers on the electrophysical characteristics of Schottky barrier diodes (SBDs). The mean crystallite size of the Mo nanostructure is computed by X-ray diffraction (XRD) spectroscopy. The I-V data is used to derive the electrical properties of these structures. These diodes' current conduction mechanisms (CCMs) and energy-dependent distributions of surface states (N_{ss}) are obtained. By reducing the ideality factor (n), series resistance (R_s), N_{ss}, and leakage current (I_0), as well as raising R_{sh} together with barrier height (BH), the usage of PVC and Mo-doped PVC interfacial polymer layers improves the performance of SBDs. Capacitance/conductance-frequency (C/G-f) measurements are used to study the dielectric constant (ε′)/loss (ε″) and ac electrical conductivity (σ_{ac}) in a wide frequency range. The negative capacitance/dielectric origin at low frequencies is thoroughly discussed.

1 Introduction

Electronic and optoelectronic devices, including Schottky barrier diodes (SBDs), solar cells (SC), photodiodes, field-effect transistors (FETs), and transistors, depend heavily on their metal/semiconductor (MS) contacts or structures [1–3]. The density distribution of interface states (N_{ss}), series resistance (R_s), doping concentration of atoms in the semiconductor bulk, frequency, interlayer thickness, and permittivity all often have an impact on how well these structures work. Recently, researchers have been trying to replace the MS structures by the metal-polymer-semiconductor (MPS) configuration to improve the performance of

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these devices. It must be notice that the polymers have a few benefits, including low cost, simple growth, high strength, and easy processing [4]. However, one of the major drawbacks of polymers is their poor conductivity, which may be greatly increased by doping certain metal atoms and metal oxide molecules [5].

Today, the primary challenge is to enhance the performance of electronic devices, such as Schottky-type diodes/photodiodes, capacitors, and solar cells, by utilizing a new high-dielectric interfacial layer between the semiconductor and gate metal, rather than the classic oxide/insulator layers grown by traditional methods. In addition, both the reliability and stability of these devices are closely related to their surface conditions, an understanding of surface physics, the homogeneity of doping atoms in the semiconductor, the nature of the barrier height (BH) and interfacial layer, fabrication processes, and the voltage applied to the device, among other factors [2–8]. Although many studies were conducted on these devices, there is still no clear consensus on their possible charge-transport/conduction mechanism (CTMs, CMs), the nature of the BH at the junction. For instance, the basic electrical parameters are usually calculated according to the standard thermionic emission (TE) theory, but they are generally deviations from the pure TE theory due to the existence of interface traps, interfacial layer, barrier inhomogeneity, highly doped donor/acceptor atoms, and series resistance (R_s). However, R_s and interlayer are more effective at the accumulation zone at high frequencies, whereas N_{ss} and polarization processes are more successful in the depletion region at low frequencies [1–6]. It is believed that the use of an organic interlayer or some of its composites instead of conventional insulators leads to improving the performance of electronic devices due to their high surface-area to volume rate, low cost/weight, good mechanical-strength, charge-storage capacity, flexibility, and easy/simple preparation methods like electrospinning, sol–gel and template synthesis [3–7].

It is well known that in addition to SBDs, the other types of diodes, such as photodiodes, PIN photodiodes, and phototransistors, are also considerably influenced by the illumination, frequency, temperature, and voltage [9–12]. For example, Buqing et al. have investigated monolithically integrated InAs/GaAs quantum dot lasers on a Si wafer with high-quality GaAs and Ge materials as buffer layers. They show that the room temperature continues wave was lying at 1320 nm, with a minimum threshold-current density of 122 $A.cm^{-2}$ and a maximum output-power of 153 mW at 10 ℃ [9]. Yuanhao Miao et al. have reviewed the recent research progress for the mesa- and planar-geometry InGaAs avalanche photodiodes, which are commonly grown by the molecular beam epitaxy or metal–organic chemical vapor deposition technique on the InP substrate [10]. Jiahan Yu et al. have also introduced the resonant-cavity-enhanced Ge PIN photodetectors on the 200 mm distributed Bragg reflector mirror; both wafers and detectors were processed by the standard Complementary Metal–Oxide–Semiconductor technology. At a bias voltage of -1 V, average responsivities were equal to 0.67 A/W at 1550 nm and 0.85 A/W at 1310 nm due to the combined function of poly-Si/SiO_2 DBR mirror and high-quality Ge absorber [11]. A. Ali Alarabi et al. used various heterojunction arrangements to extract some characteristics of vertical p-n and p-i-n photodiodes with the p-PMItz organic semiconductor. Experimental findings have demonstrated that the same organic semiconductor has exhibited different results in distinct layer and anode contact (Ag and In) configurations. These results not only validate the effectiveness of the proposed configurations but also highlight the potential for future applications in sensor technology [12].

Recent studies, for instance, have revealed the existence of negative dielectric (ND) and negative capacitance (NC) in several electronic devices, including MS and MPS-type contacts [13–15], PN junctions [8], photo and far-infrared detectors [12], light-emitting diodes (LEDs) [16], and hetero-configurations [17]. Because there is a lack of confidence in the experimental results, the idea of NC or ND is meaningless to us and is not often accepted [18, 19]. As a result, anomalous or aberrant conduct is frequently used to describe the NC or ND incident that has been documented in the literature [20]. Due to the saturation impact of interface trap levels at the transition frequency, the value of C may quickly shift from negative to positive values at low frequencies. Almost no traps or states may follow the alternating ac signal because as the frequency grows, the relaxation/lifetime exceeds the period (T = 1/2f) or the alternating ac signal. As a result, C goes back to positive values and gets closer to the sample's typical geometrical capacitance. Put differently, trap and polarization contributions to the observed C can be disregarded for middle/large frequencies [17, 21]. According to Butcher et al. [22] and Huang et al. [23], instrumental issues such as parasitic inductance or incorrect calibration of measuring equipment are the

cause of NC. Zhu et al. [24] said in a distinct study that the junction's C is the differential impact of electric charge (Q) with respect to junction voltage V_j ($C = dQ/dV_j$), resulting in observation of NC.

For the reasons explained above, in this work, we employed Polyvinyl-chloride (PVC) polymer for preparing of interface layers. It should be mentioned that PVC is a thermoplastic polymer with remarkable insulating properties. Elastic moduli of PVC, in both its stiff and soft forms, range from 1500 to 3000 MPa. It can be heated to 260 ℃ by adding a heat stabilizer, even though its melting point is 100 ℃. PVC is an excellent material to use for low voltage and frequency insulation because of its dielectric constant, volume resistivity, and large dielectric loss tangent [25]. Molybdenum (Mo) is a transition metal with atomic number 42 and is found in group 6 of the periodic table [26]. Its atomic structure features a single electron in its outermost shell, which contributes to its high melting point of 2,623 ℃ (4,753 °F) and density of 10.28 g/cm^3 [27]. Molybdenum has a silvery-gray metallic appearance, and its crystal structure is body-centered cubic (BCC). Its oxidation states primarily include −2, 0, + 2, + 3, + 4, + 5, and + 6, with + 6 being the most stable in compounds. Molybdenum occurs naturally in various minerals, most notably molybdenite (MoS_2), and is mainly extracted through sulfide ore processing [28]. In addition, molybdenum's unique properties, such as its excellent resistance to corrosion and ability to retain strength at high temperatures, make it essential in various industrial applications [29]. It is widely used in alloying steel to enhance hardness, strength, and resistance to wear and corrosion, often found in high-strength steel grades. Therefore, it serves crucial roles in the production of aircraft components, military applications, and tools that require high durability [30]. In the electronics industry, it is used for electrical contacts and as a filament in light bulbs and high-temperature vacuum tubes. Furthermore, molybdenum compounds have significant roles in chemical catalysts and as a component in lubricants, showcasing their versatility in both manufacturing and technological advancements [31, 32].

For usage in interfacial layer electric and dielectric applications, our goal is to characterize the PVC and PVC:Mo interlayers with the I-V and C/G-f measurements. To achieve this, three types of SBDs or structures—known as Au/n-Si (C_0), Au/PVC/n-Si (C_1), and Au/PVC: Mo/n-Si (C_2)—are provided on the same n-type Si wafer under the same circumstances. XRD spectroscopy is applied to examine the average crystallite size of the Mo nanostructure. Next, some of their primary electrical parameters—I_0, n, BH, R_{sh}, and R_s—are extracted from the I-V data based on thermionic emission (TE) theory, modified Norde method, and Cheung functions. Then, the Card-Rhoderick approach is utilized to derive the energy-dependent profile of N_{ss} from the I-V data at the forward-bias zone. Moreover, the plot of the $Ln(I_F)$-$Ln(V_F)$ at the forward bias and $Ln(I_R)$-$V_R^{0.5}$ in the reverse bias is used to calculate their current conduction mechanisms (CCMs). Both PVC and PVC:Mo interlayers result in a drop in the n, R_s, N_{ss}, I_0 and an increase in the R_{sh}, BH, RR when the electrical properties of the MPS and MS structures are compared. These findings support the idea that MPS architectures perform better. Ultimately, the frequency-dependent profiles of ε′, ε″, tanδ, R_s and σ_{ac} of these structures are derived from the measured C/G-f data at wide-range frequency (100 Hz-1 MHz). The observation of negative capacitance/dielectric at low frequencies is thoroughly examined.

2 Experimental procedure

2.1 Materials and devices

Several substances were employed in this work, including distilled water, n-type silicon wafer, acetone (CH_3COCH_3), hydrogen peroxide solutions (H_2O_2), and Mo nanopowder. To ascertain the average crystallite size of the Mo sample, XRD spectrometer with Cu-K_α radiation in 15.5 nm wavelength (model: Philips X-Pert) was employed. It should be noted that the voltage dependency of electric current (I-V) on a voltage range of ± 3.2 V and frequency-dependent capacitance (C–f) over an extent frequency range of 100 Hz-1 MHz were measured using KEITHLEY (2450) and KEYSIGHT impedance analyzer (E4980Al 20 Hz-1 MHz), respectively.

2.2 The fabrication steps of SBD structures

These three structures were made using n-Si (P-doped) crystals with resistivity of 1–10 Ω.cm, (100) float zone, 300 μm thickness, and one-side polishing. First, a method we generally described in our earlier studies was used to clean the n-Si wafer [3, 4, 7]. The sputtering coating technology provided a pure Au coating for back contact. Second, an interfacial layer

was created on n-Si by applying the prepared PVC and PVC:Mo solutions to the front side of the material using the spin coating process. It was calculated that they were 100 nm thick. Lastly, Schottky contacts with an area of 0.0113 cm^2 and a thickness of 150 nm have been deposited on top of the n-Si wafer once again using the thermal evaporation method.

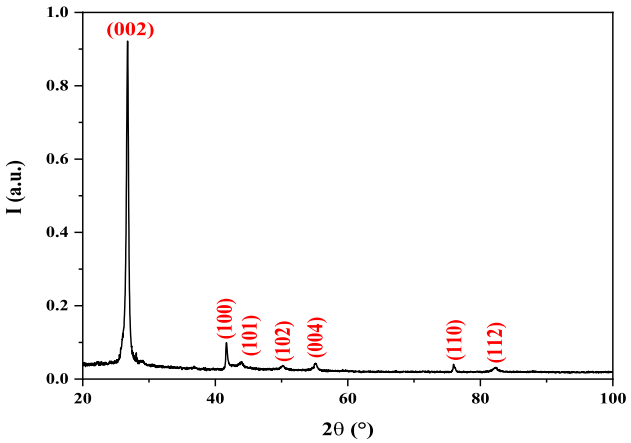

Fig. 1 XRD patterns of Mo nanoparticles

3 Results and discussion

3.1 XRD analysis of Mo nanoparticles

Figure 1 shows the XRD pattern of the Mo nanostructure that was used as a dopant in PVC polymer interlayer. The angles 2θ of 26.8°, 41.7°, 44°, 50.3°, 55.1°, 76°, and 82.4° are corresponding to the crystallite planes displayed in the XRD pattern, respectively. Furthermore, the average crystalline size is determined using the Debye–Scherrer equation, which is expressed as $D = k\lambda/\beta\cos\theta$. The variables of D, k, λ, β, and θ stand for the crystallite size, the Scherer constant (~ 0.9), the wavelength of X-ray radiation (15.4056 nm), the full width at half maximum of the XRD peak, and the Bragg angle, respectively [33]. The Debye–Scherrer equation yields an average crystalline size of 31 nm for the Mo nanostructure.

3.2 Current–voltage (I-V) measurements

Figure 2a shows the changes in the electronic current in the prepared SBDs depending on the applied voltage in a range of ± 3.2 V at room temperature. It must be mentioned that TE theory describes the movement of electronic charges (electrons/holes) with enough thermal energy over barriers. As a result, using TE

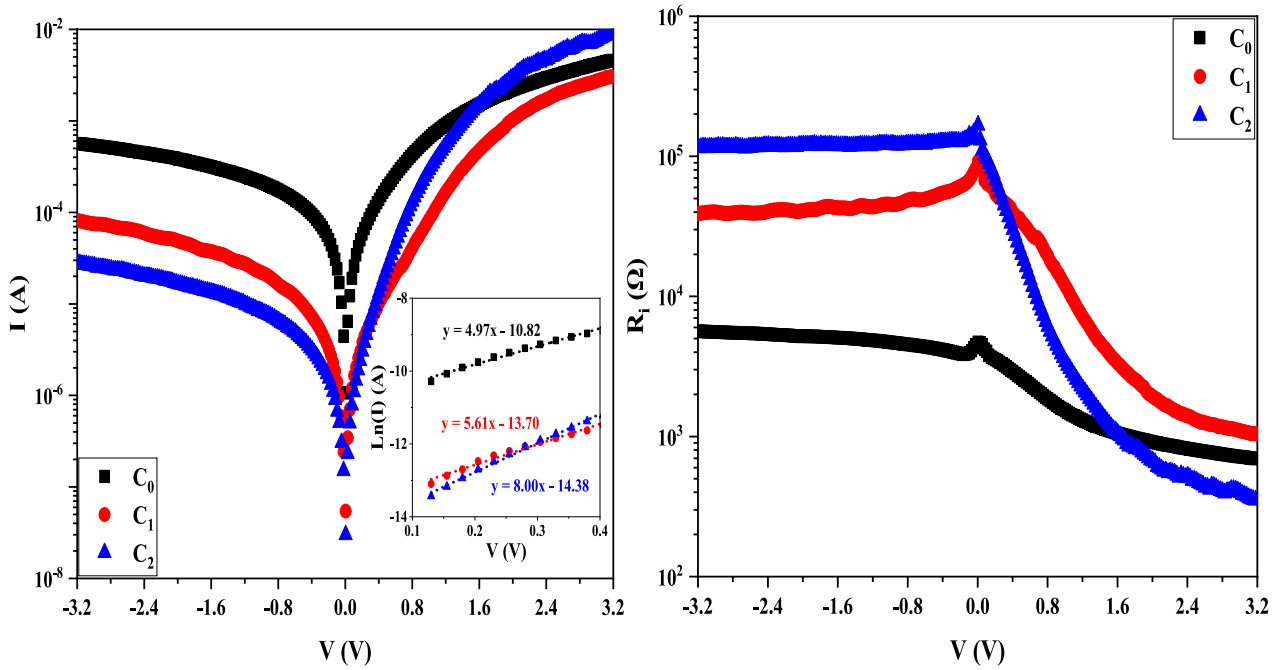

Fig. 2 The semi-logarithmic voltage-dependent plots of **a** electric current and **b** resistance for the developed samples

theory, the fundamental electrical characteristics of MS-type structures with or without an interfacial layer at the M/S interface are typically derived from the I-V data in the forward-bias region. However, because of barrier inhomogeneity at the junction, D_{it}, R_s, and the interfacial layer, they occasionally strayed from the ideal scenario. Following TE theory, the I-V relationship in MS/MPS-type structures with R_s, $n > 1$, and $V \geq 3kT/q$ is as follows [2123]:

$$I = AA^*T^2 exp\left(-\frac{q}{kT}\Phi_{B0}\right)\left[exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right] \quad (1)$$

The reverse-saturation current (I_0) is expressed in front of square brackets in this case, along with the ideality factor (n), barrier height (Φ_{B0}), Richardson-constant (A^*), which for n-type Si is equal to 112 A/(cm.K)^2, and other parameters that are widely known from the literature [2–10]. Using the rectifier contact area and the I_0 measure obtained from the Ln(I)-V graph intercept (refer to Fig. 2a) at V = 0, the quantity of Φ_{B0} may be computed as follows [2]:

$$\Phi_{B0} = \frac{kT}{q} Ln\left(\frac{AA^*T^2}{I_0}\right) \quad (2)$$

The quality of MS/MPS-type samples is represented by the value of n, which is idealistically expected to be unity (= 1). However, in practice, this value is typically more than 1 because of the presence of interlayers and their thickness (δ_i), as well as dielectric values (D_{it}) and depletion-layer width (W_D). It could be given by [23]:

$$n = \frac{q}{kT}\left(\frac{dV}{d(LnI))}\right) = 1 + \left(\frac{\delta_i}{\varepsilon_i}\right)\left\{\frac{\varepsilon_s}{W_D} + qD_{it}\right\} \quad (3)$$

Therefore, the measures of I_0, n, and Φ_{B0} are equal to 2.04×10^{-5} A, 7.73, 0.607 eV for C_0, 1.12×10^{-6} A, 6.88, 0.682 eV for C_1, and 5.57×10^{-7} A, 4.83, 0.700 eV for C_2, respectively. The rectifier ratio (RR = I_F/I_R at ± 3.2 V), which was determined to be 8.30, 38.08, and 352.27 for the C_0, C_1, and C_2 structures, respectively, is another, more significant aspect that affects how well the MS/MPS-type structures work. The RR value for C_2 is 42 times greater than that of the MS structure. Moreover, Ohm's law was used to get the resistance ($R_j = dV_j/dI_j$) against V profiles of the fabricated constructions. As shown in Fig. 2b, the resistance at high forward voltage (3.2 V) corresponds to the true value of R_s, while at low reverse voltage (−3.2 V), it relates to R_{sh}. The measure of R_s is found to be 0.69 kΩ for C_0, 1.03 kΩ for C_1, and 0.33 kΩ for C_2, respectively. Also, the R_{sh} value for C_0, C_1, and C_2 structures is 5.67 kΩ, 38.94 kΩ, and 114.22 kΩ, respectively.

Next, Cheung functions are used to derive the fundamental electric factors of the developed structures (n, R_s, and Φ_{B0}) using the deviation of the linear component of Ln(I)-V profiles as [34, 35];

$$\frac{dV}{d(LnI)} = IR_s + \left(\frac{nkT}{q}\right) \quad (4)$$

$$H(I) = V - \frac{nkT}{q} Ln\left(\frac{I}{AA^*T^2}\right) = IR_s + n\Phi_B \quad (5)$$

Cheung functions state that the slopes and intercepts linear sections of the dV/d(lnI)-I and H(I)-I plots (see Fig. 3a, b) might be employed to get the measures of n, R_s, and Φ_{B0}. Both the experimental results of n, R_s, and Φ_{B0} obtained by Cheung functions and TE theory at RT are listed in Table 1.

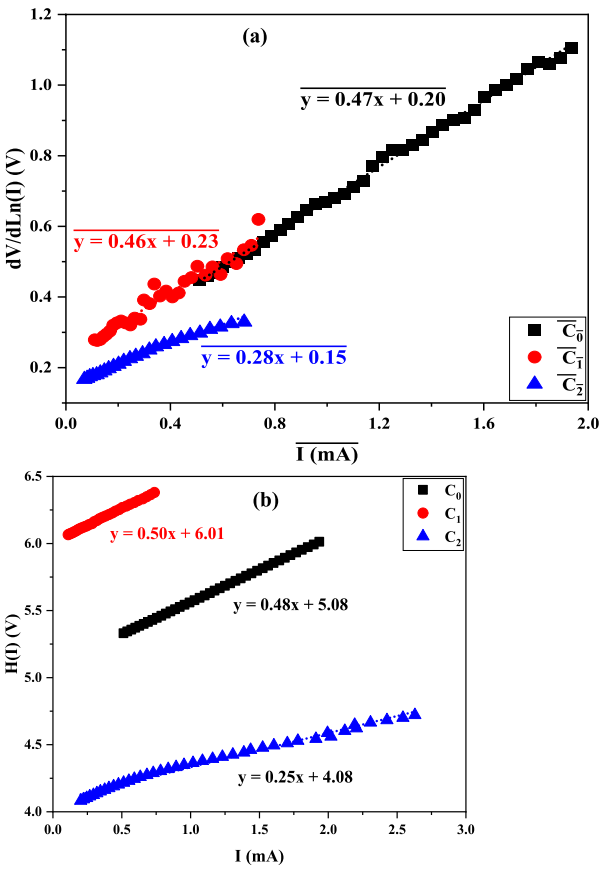

Fig. 3 Variations of **a** dV/dln(I) and **b** H(I) plots depending on electronic current for the prepared samples

Table 1 Electric variables of the developed SBDs according to various techniques

Diode	Φ_{B0} (eV)			RR	R_s (kΩ)				R_{sh}(kΩ)	n	
	TE	Norde	H(I)		TE	Norde	H(I)	dV/dLn(I)		TE	dV/dln(I)
C_0	0.607	0.598	0.625	8.30	0.69	0.65	0.47	0.48	5.67	7.73	8
C_1	0.682	0.661	0.678	38.08	1.03	0.95	0.46	0.50	38.94	8.85	6.89
C_2	0.700	0.705	0.705	352.27	0.33	0.36	0.28	0.25	114.22	4.83	5.77

Another method for determining the BH and R_s measures for the C_0, C_1, and C_2 diodes is to use the Norde function, F(V), which is represented as [35]:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}[Ln(\frac{I(V)}{AA^*T^2})] \quad (6)$$

where an integer greater than n is denoted by γ. Figure 4a shows the variations of F(V) with respect to V for three SBD structures. Figure 4a shows a concave portion that corresponds to the minimum point of F(V). Noteworthy, the Norde function minimal [35] can be used to calculate the Φ_{B0} and R_s, which are likewise introduced in Tab. 1.

In general, one of the key variables influencing the non-ideality behavior of the SBD structures is the density of D_{it} or N_{ss}. However, by taking into account the voltage-dependent BH and n, the energy-dependent density distribution of interface/trap states in the developed samples might be derived from I-V data at the forward-bias region. The distribution of N_{ss} at the equilibrium state could be determined as follows [2, 23]:

$$N_{ss}(V) = \frac{1}{q}[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_D}] \quad (7)$$

where W_D refers to the depletion-layer width, measured at 0.0113 cm^2, and δ is the interlayer thickness, which is equivalent to 100 nm. Furthermore, the electric permittivity of the semiconductor and interlayer are represented by ε_s and ε_i, respectively. For n-type semiconductors, the energy distinction between the conduction band edge (E_c) and the N_{ss} level (E_{ss}) can be expressed as: $E_c - E_{ss} = q(\varphi_e - V)$ [2, 23]. The profile of N_{ss} relies on energy differences for the three manufactured structures is represented in Fig. 4b. As can be observed, the highest values of 2.94×10^{13} $eV^{-1}.cm^{-2}$ for the C_2 sample and 4.54×10^{13} $eV^{-1}.cm^{-2}$ for the C_1 structure are lower than the value of N_{ss} for C_0, which is equivalent to 7.97×10^{13} $eV^{-1}.cm^{-2}$. Because of the polymer and nanocomposite interlayers in their

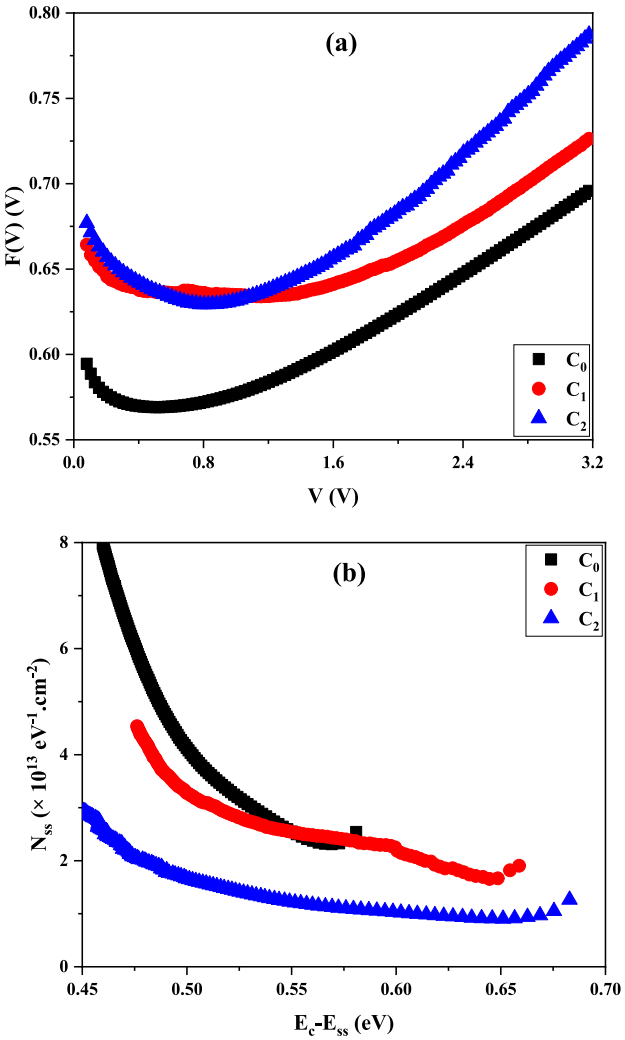

Fig. 4 Changes in **a** F(V) depending on voltage and **b** N_{ss} versus energy for the manufactured samples

configurations, which cause semiconductor surface passivation, the maximum value of the N_{ss} profiles for C_1 and C_2 diodes is smaller than that of the C_0 diode [36, 37].

In summary, Tab. 1 presents the key electrical parameters for the C_0, C_1, and C_2 structures that were

determined using conventional TE theory, modified Norde, and Cheung formulations. It is evident that the presence of PVC and PVC:Mo interfacial layers cause the BH of the C_1 and C_2 samples to be relatively higher than that of the C_0 structure. Additionally, the C_2 diode has a lower R_s compared with the C_0 structure while the R_s of the C_1 sample is slightly higher. On the other hand, the growth of the R_{sh} of the C_1 and C_2 structures is observed about by the insertion of an interfacial layer into the C_0 structure, both with and without doping Mo content. It should be noted that the RR value of C_2 is much higher than that of C_0 and C_1 structures where Mo is doped into the PVC polymer layer. Moreover, the interfacial layer is used to reduce the value of n which has been achieved by PVC:Mo nanocomposite. Therefore, adding Mo nanostructures to the PVC polymer layer improves the C_2 diode's performance by raising RR, BH, $R_{sh,}$ and declining leakage current, n, R_s. The values that were computed using different methods accord well with one another.

Additionally, studies at forward and reverse biases have examined the effects of PVC and PVC:Mo thin layers on the current conduction processes and the free carriers current of the C_0, C_1, and C_2 SBDs. Figure 5a depicts the $Ln(I_F)$-V_F profiles of the developed structures including several areas corresponding to various CCMs. Charge transfer is generally improved by the formation of deep traps at the contact. The slopes of the two linear sections on the graph of the C_0 structure are 1.16 and 1.72. In addition, the three linear sections of the C_1 and C_2 diodes have slopes of 1.25, 1.78, 3.21, and 1.35, 2.74, 3.13. At the first area of the graphs, which corresponds to the slope's near unity, an ohmic behavior (I ~ V) is seen. Owing to the low bias voltage in this area, the electrodes inject modest charges into the semiconductor [37]. Because recombination-tunneling is the dominating CCM, the slope of the second section of the C_2 profiles is more than two, and the current varies exponentially (I ~ exp(cV)) [38]. It can be observed that the current varies as a power function ($I \sim V^m$) in the third part of the C_2 plot due to the space charge limited current (SCLC) process [37, 38].

To examine the CCMs of C_0, C_1, and C_2 diodes, one of two processes may occur at the reverse bias voltage: either Poole–Frenkel emission (PFE) or Schottky emission (SE). Once PFE process dominates, the quantity of I_R is defined as [39],

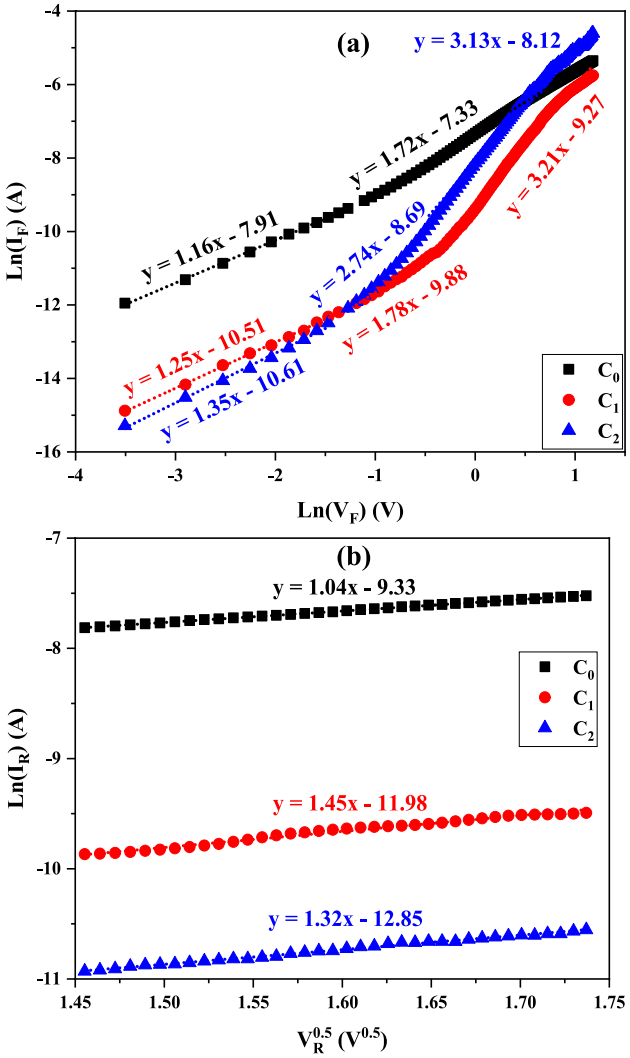

Fig. 5 Profiles of **a** $Ln(I_F)$-V_F and **b** $Ln(I_R)$-$V_R^{0.5}$ for the C_0, C_1, and C_2 structures

$$I_R = I_0 exp(\frac{\beta_{PFE} V^{0.5}}{KTd^{0.5}}) \quad (8)$$

the I_R is formulated by the following relation provided that the SE mechanism is predominant,

$$I_R = AA^* T^2 exp(-\frac{\Phi_{B0}}{kT}) exp(\frac{\beta_{SE} V^{0.5}}{KTd^{0.5}}) \quad (9)$$

In this case, $2\beta_{SE} = \beta_{PFE}$ represents the relationship between the field lowering coefficients for the PFE mechanism (β_{PFE}) and the SE mechanism (β_{SE}) [40].

The $Ln(I_R)$ fluctuations for the C_0, C_1, and C_2 diodes are illustrated as a function $V_R^{0.5}$ in Fig. 5b. It is clear that the graphs of these three diodes have linear behavior. Consequently, the field

lowering coefficients were 3.22×10^{-6} $eV^{-1}m^{0.5}V^{0.5}$ for the C_0, 1.07×10^{-5} $eV^{-1}m^{0.5}V^{0.5}$ for the C_1, and 1.15×10^{-5} $eV^{-1}m^{0.5}V^{0.5}$ for the C_2 based on the slope of these linear areas. For the C_0, C_1, and C_2 structures, the theoretical findings of β_{PFE} were found to be 3.86×10^{-5} eV.

$^{-1}m^{0.5}V^{0.5}$, 1.02×10^{-5} $eV^{-1}m^{0.5}V^{0.5}$, and 1.13×10^{-5} $eV^{-1}m^{0.5}V^{0.5}$, respectively. The CCM into the C_1 and C_2 diodes is the PFE mechanism, according to a comparison of the theoretical and experimental data.

3.3 Impedance characteristics

In order to investigate the impact of the PVC and PVC:Mo interlayers on the capacitive feature of the C_0 diode, the frequency-dependent impedance of the C_0, C_1, and C_2 structures has been studied at the DC bias voltage of 1.5 V and frequency range 100 Hz-1 MHz. At room temperature, the capacitance fluctuations for the C_0, C_1, and C_2 structures are shown in terms of frequency (C–f) in Fig. 6a–c. These diodes' frequency-dependent capacitance varies exponentially because of the dispersion effect, which prevents charges in interface states and in equilibrium with semiconductors from affecting capacitance at higher frequencies. Consequently, they do not follow the AC signal [41, 42]. Furthermore, the G/ω-f graphs can be used to specify the energy distribution of interface states. Figure 6 shows the changes in G/ω with respect to frequency. It should be noted that at higher frequencies, the electrical dipole moments are unable to obey the electric field, which results in a decrease in G/ω as frequency increases.

The permittivity of diodes is a significant dielectric characteristic. It is often expressed as a complex quantity, $\varepsilon^* = \varepsilon\prime - j\varepsilon''$. The stored energy was represented by the real part, $\varepsilon\prime = C/C_0 = Cd_i/\varepsilon_0 A$, and the loss energy was represented by the imaginary part, $\varepsilon'' = G/\omega C_0 = Gd_i/\varepsilon_0 \omega A$, where $C_0 = \varepsilon_0 A/d_i$ denotes the geometric capacitance of the samples, and ε_0, A, and d_i are the permittivity of free space, the rectifier contact area of the samples, and the thickness of the interfacial polymer layer, respectively [43].

In this manner, the frequency variations of ε′ at 1.5 V DC bias voltage and room temperature are displayed in Fig. 7a–c. As can be observed, the plots tend to become constant with increasing frequency after reaching a minimum value at 200 Hz. The minimum value of C_0 is decreased to −5.49 and −44.93, respectively, by introducing both the PVC and

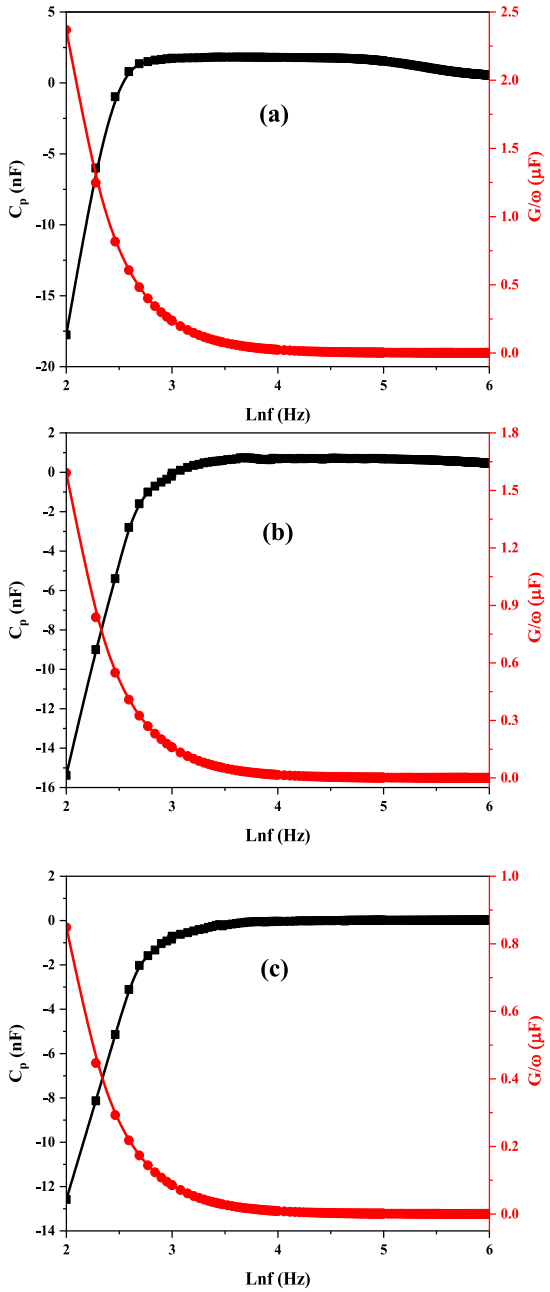

Fig. 6 Semi-logarithmic frequency-dependent plots of the C and G/ω **a** C_0, **b** C_1, and **c** C_2 structures

PVC:Mo thin layers at the M/S interface. The dielectric constant of C_1 sample with PVC interfacial layer is slightly larger than that of for C_2 structure whose interlayer is PVC:Mo nanocomposite at higher frequencies even if they reduce the MS diode's stored energy at 200 Hz.

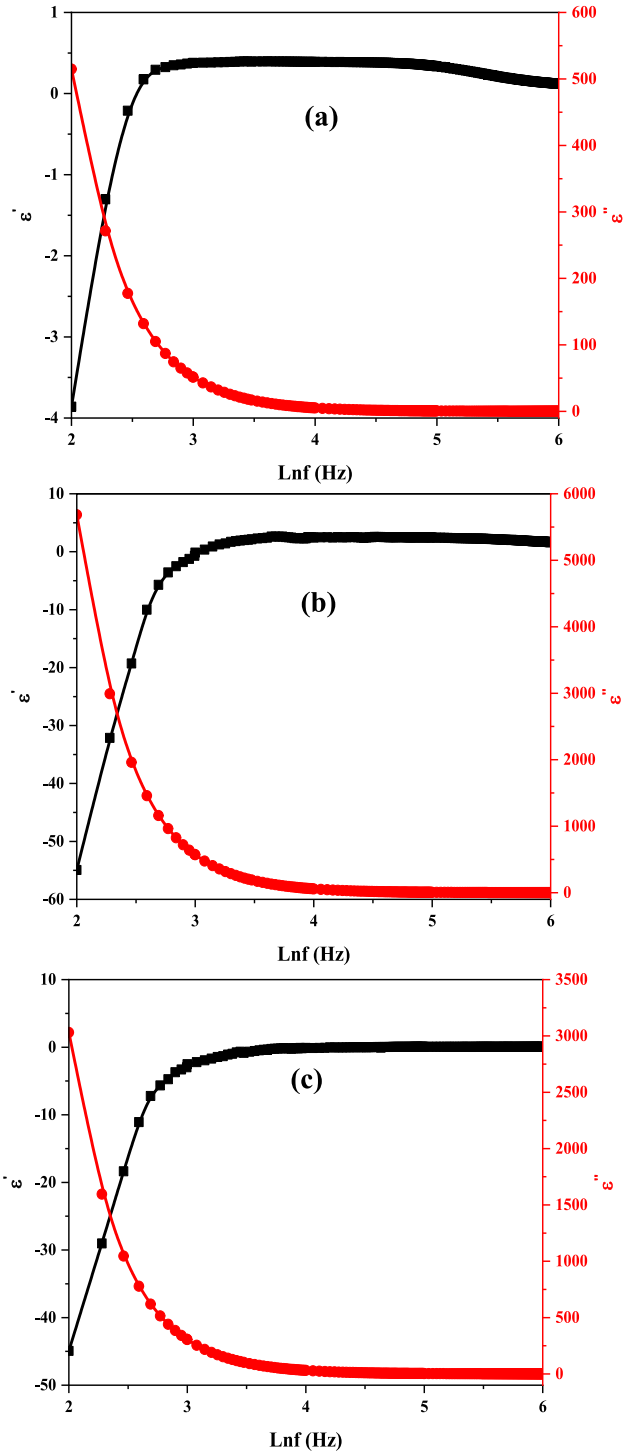

Fig. 7 Semi-logarithmic frequency-dependent profiles of ε' and ε'' for **a** C_0, **b** C_1, and **c** C_2 structures

Additionally, Fig. 7 shows the changes in the imaginary portion of complex permittivity, as a function of frequency at an ambient temperature and a DC bias

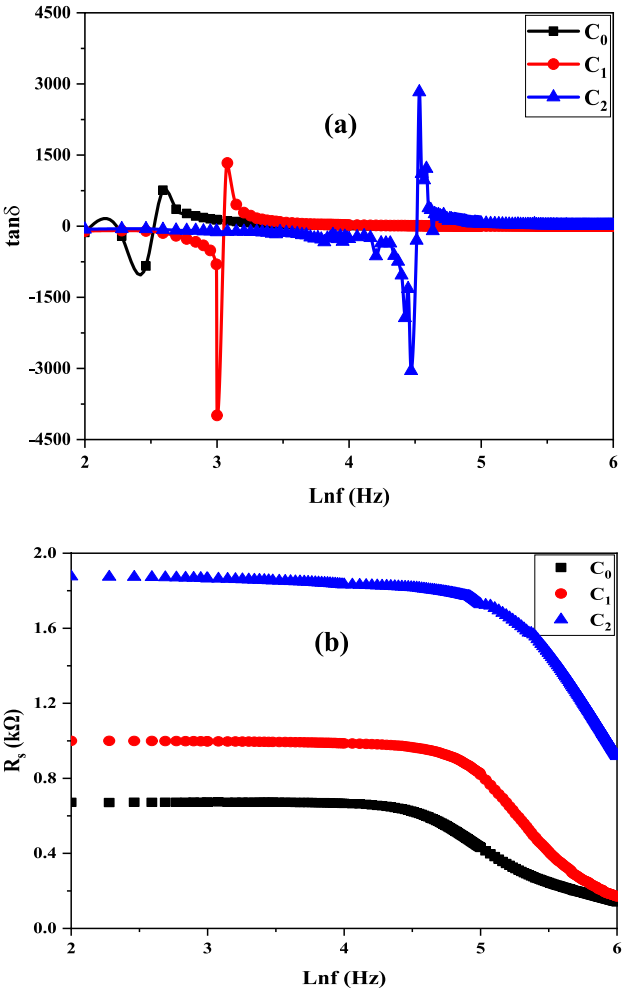

Fig. 8 Semi-logarithmic frequency-dependent profiles of **a** tanδ and **b** R_s for the prepared structures

voltage of 1.5 V. The behavior of the C_0, C_1, and C_2 structures is consistent over the frequency range, as can be observed. The usage of PVC and PVC:Mo thin film increases the lost energy in the C_1 and C_2 diodes as respect to the C_0 structure at a frequency of 200 Hz. But by raising the frequency, the interfacial layer presence effect is removed, and each sample's lost energy is lowered to a comparable constant value. Major responses of C_0, C_1, and C_2 structures appear at lower frequency due to the high resistive nature of the grain boundary [40].

The quick change in the value of C from negative to positive values, as shown in Figs. 7 and 8, can be ascribed to the saturation impact of interface trap levels at low frequency transition frequency. Stated otherwise, the greatest value of C and G, respectively, corresponds to the minimum value of the NC and ND

constants. Their actions are referred to as inductive conduct. However, at higher frequencies, the relaxation time is greater than T(= 1/2f), making it nearly impossible for traps to follow the ac signal. As a result, C value goes back to positive values and gets closer to the sample's typical geometrical capacitance. Such negative capacitance or negative dielectric behavior is attributed to instrumental issues by Butcher et al. [22] and Huang et al. [23].

Zhu et al. [24] state that the junction capacitance, or $C = dQ/dV_j$, is the differential impact of electronic charges (Q) with regard to junction voltage V_j. Some researchers have recently published similar findings [5–8, 10–14], However, due to a lack of confidence in the experimental results, the reported NC and ND constant at lower and higher frequencies could not represent anything to us or be widely recognized [14–19]. We conclude that the observed NC and ND at low frequencies are caused by polarization and interface traps, whereas series resistance is responsible for them at higher frequencies.

Additionally, tanδ is an electrophysical characteristic that may be expressed as $tan\delta = \varepsilon''/\varepsilon' = G/\omega C$, where δ denotes the phase difference between the induced current and the applied electric field [43, 44]. Figure 8a shows the variations in tanδ as a function of frequency at 1.5 V DC bias voltage and room temperature. The plots of the C_0, C_1, and C_2 structures show strong peaks at the positive and negative half-planes of tanδ. The observed NC at these frequencies also contributes to the reported negative value in the tanδ. High resistance at lower frequencies might induce the grains and smile border. Furthermore, at higher frequencies, grain resistance decreases. To transport the charge carriers at lower frequencies, however, more electrical energy is needed, and vice versa. These are the outcomes of the frequency-dependent decrease in tanδ.

It should be mentioned that using a semiconductor material with a high dopant content or lowering the barrier height at the metal–semiconductor interface lowers the series resistance. Based on the Nicollian and Brews approach, the variations of series resistance, R_s, in terms of frequency are defined as follows [45]:

$$R_s = \frac{G}{G^2 + (\omega C)^2} \tag{10}$$

where C and G/ω represent the capacitance and conductance experimental data at any bias voltage. Moreover, the variations in the R_s profile with respect to frequency at room temperature and DC bias voltage are displayed in Fig. 8b. At lower frequencies, the R_s value for the C_0, C_1, and C_2 structures remains constant; however, at higher frequencies, it decreases. This is because the charges at interface traps may follow the AC signal at low and moderate frequencies, which allows them to contribute to both series resistance and the actual value of the traps. In general, The R_s value has a significant effect on the C-V and G/ω-V characteristics for enough high frequencies in the accumulation region as well as I-C characteristics in the enough high forward-bias region. According to Nicollian and Brews [1], the R_s can originate from several reasons such as the back-ohmic & front rectifier-contact, the bulk resistivity of the semiconductor, the impurities on the film, and extraordinarily nonuniform-doped acceptor or donor atoms (N_a, N_d) within the semiconductor. Having a lower barrier height (BH), heavily doped semiconductors, or a thin depletion-layer width leads to tunneling through the barrier. At lower frequencies, the value of period ($T = 1/2\pi f$) becomes higher than the lifetime of surface states (τ), which are localized at the interlayer/semiconductor interface in the bandgap of the semiconductor and hence can supply an excess conductance (G_{ex}) to the measured real value of G(= 1/R). A better fabrication and cleaning process, low frequency C/G-V measurements, and adjusted/corrected C/G-V plots can considerably reduce the R_s effect.

The electrical conductivity, σ_{ac}, is the last frequency-dependent property of the C_0, C_1, and C_2 diodes which have been investigated in the current work. It is defined as follows [46]:

$$\sigma_{ac} = (\frac{d_i}{A})\omega C tan\delta = \varepsilon''\omega\varepsilon_0 \tag{11}$$

Electrical conductivity often follows the power law in the manner given by [47]:

$$\sigma_{ac} = \sigma_0 + A\omega^{f_1} + B\omega^{f_2} \tag{12}$$

In the context of ac electrical conductivity, σ_0 represents the DC component, $\omega = 2\pi f$ denotes the angular frequency, and f_1 and f_2 are dimensionless frequency exponents that provide more details on the conduction mechanisms inside the C_0, C_1, and C_2 structures. The f_1 and f_2 parameters are obtained from the slope of the

Ln(σ_{ac})-Ln(ω) figure. Figure 9a illustrates how the ac electrical conductivity changes at room temperature in relation to frequency. The AC electrical conductivity increases because of a decrease in interfacial polarization at higher frequencies. By raising the σ_{ac}, which causes a drop in series resistance, the eddy current and energy loss increase [25, 47].

The ac electrical conductivity of the C_0, C_1, and C_2 structures is constant because the DC component of the ac electrical conductivity has a greater impact at lower frequencies. For the C_0, C_1, and C_2 diodes, the figure of Ln(σ_{ac}) in terms of Ln(ω) is shown in Fig. 9b. The Ln(σ_{ac})-Ln(ω) plots of the C_0, C_1, and C_2 diodes clearly show two linear areas with different slopes. The slope of the second linear areas of the prepared samples is equal to 0.35, 0.48, and 0.44 for the C_0, C_1, and C_2 diodes, respectively, even if the *f* value in the first linear region of the SBDs is the same. As can be observed, because of the interaction of the charge carriers with the trap states at great frequencies, the slope of the second linear parts of the C_0, C_1, and C_2 diodes is between 0 and 1 [48].

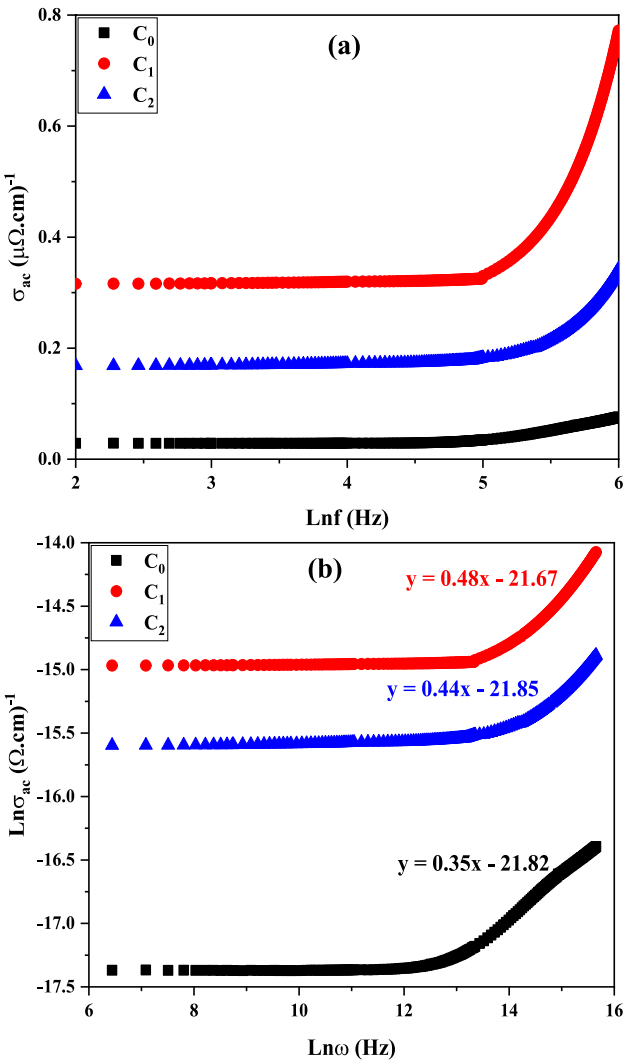

Fig. 9 **a** semi-logarithmic frequency-dependent σ_{ac} and **b** Ln(σ_{ac})-Ln(ω) profiles for the C_0, C_1, and C_2 structures

The electrical parameters and dielectric characteristics are all demonstrated by these findings [49]. However, R_s and interlayer are more effective at the accumulation zone at high frequencies, whereas N_{ss} and polarization processes are more successful in the depletion region at low frequencies [1–5]. The observed low frequency of NC, where the value of C rapidly shifted from negative to positive values, can be explained by the interface trap levels at the transition frequency reaching saturation. However, when the frequency rises, the lifetime surpasses the period ($T = 1/2f$), meaning that nearly no traps are unable to track the ac signal. As a result, the value of C goes back to positive values and gets closer to the structure's typical geometrical capacitance. As a result, there is still no clear consensus on the possible charge-transport/conduction mechanism (CTMs, CMs), the nature of BH at the M/S interface, and NC behavior in the electronic devices. In the literature, the basic electrical parameters are usually calculated from the thermionic emission (TE) theory, but they are usually deviated from this theory due to the existence of interface traps/states, interfacial layer, barrier inhomogeneity, highly doped donor/acceptor atoms, series resistance (R_s), etc. [50–52]. It is believed that the use of a high-dielectric interlayer instead of conventional insulators, such as SiO_2 leads to an increase in the performance of these devices. As seen from Eq. 5, the dielectric and W_d values of the interface layer are inversely proportional to ideality factors, while they are directly proportional to N_{ss}. Therefore, when high-dielectric interface layers are used, the n value will approach the ideal case ($n = 1$). Similarly, a high-dielectric interface layer will increase the capacitance value, especially at low frequencies, allowing many electronic charges or energy to be stored in the capacitor. Because at low frequencies ($T \geq \tau$), interface traps and dipoles have enough relaxation or lifetimes (τ) that will easily follow the ac signal and easily rotate around its axis in the direction of the electric field. In this case, the charges at traps and dipole will be supplied with an excess capacitance and conductance to their real values.

4 Conclusions

In this study, three SBDs were manufactured by the same n-type Si wafer: Au/n-Si (C_0), Au/PVC/n-Si (C_1), and Au/PVC:Mo/n-Si (C_2). First, XRD spectroscopy was employed to compute the average crystallite size of the Mo nanostructures that was found to be 31 nm. Next, using several mathematical techniques (TE hypothesis, modified Norde, and Cheung functions), the fundamental electrical properties of the developed structures (I_0, BH, n, R_s, and R_{sh}) were extracted from the I–V data and compared to one another at room temperature. They were found to be 2.04×10^{-5} A, 607 eV, 7.73, 0.69 kΩ, 5.67 kΩ for C_0, 1.12×10^{-6} A, 0.682 eV, 6.88, 1.03 kΩ, 38.94 kΩ for C_1, 5.57×10^{-7} A, 0.700 eV, 4.83, 0.33 kΩ, 114.22 kΩ for C_2 structures. It is evident that the measures of I_0, R_s, and n decrease with PVC and PVC:Mo polymer interlayers, whereas the values of BH and R_{sh}. In addition, RR for C_2 is greater than RR for C_1 and C_0 structures. Additionally, because polymer/nanocomposite thin films prevent semiconductor surface passivation, the density of D_{it} for C_0 diode is decreased. The forward- and reversed-bias CCMs of C_0, C_1, and C_2 samples were examined. The CCM into C_1 and C_2 SBDs are PFE mechanisms based on a comparison of the theoretical (1.02×10^{-5} $eV^{-1}m^{0.5}V^{0.5}$ for the C_1 and 11.13×10^{-5} $eV^{-1}m^{0.5}V^{0.5}$ for the C_2) and experimental (1.07×10^{-5} $eV^{-1}m^{0.5}V^{0.5}$ for the C_1 and 1.15×10^{-5} $eV^{-1}m^{0.5}V^{0.5}$ for the C_2) findings of the β_{PFE} factor.

Eventually, the dielectric characteristics of the fabricated structures have been studied with respect to their frequency dependency by measuring the impedance at 1.5 V bias voltage in the 200 Hz-1 MHz frequency range. The quantity of C and G/ω, or ($\varepsilon\prime$ and $\varepsilon\prime\prime$) was shown to be significantly altered at lower frequencies and to become nearly frequency-independent at higher frequencies. Furthermore, by enhancing interfacial polarization and lowering the R_s, the ac electrical conductivity for MPS SBD was enhanced at higher frequencies in comparison to the MS structure. While σ remains constant at lower frequencies, it begins to increase at higher frequencies, which are associated with dc and ac conductivity, respectively. Three factors were identified as the cause of the observed negative dielectric constant or capacitance at lower frequencies: the presence of the polymer/nanocomposite interfacial layer, the saturation impact of interface trap levels at transition frequency, and the difference in electric charge (Q) with regard to C = dQ/dV. In literature, "inductive" behavior is defined as the minimum measure of C matching the maximum value of G/ω.

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Author contributions

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Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Declarations

Conflict of interest The authors declare no financial or commercial conflict of interest.

Ethical approval Not applicable.

Consent to participate Not applicable.

Consent for publication Not applicable.

References

1. Nicollian EH, Brews JR. MOS (metal oxide semiconductor) physics and technology. John Wiley & Sons; 2002.
2. Sze SM, Li Y, Ng KK. Physics of semiconductor devices. John wiley & sons; 2021.
3. A.D. Tataroglu, A. Buyukbas Ulusan, Ş Altındal, Y.A. Azizian-Kalandaragh, A compare study on electrical properties of MS diodes with and without $CoFe_2O_4$-PVP interlayer. J. Inorg. Organomet. Polym. Mater. **31**, 1668–1675 (2021)

4. S.A. Yerişkin, M. Balbaşı, İ Orak, The effects of (graphene doped-PVA) interlayer on the determinative electrical parameters of the Au/n-Si (MS) structures at room temperature. J. Mater. Sci. Mater. Electron. **28**, 14040–14048 (2017)
5. M. Sharma, S.K. Tripathi, Frequency and voltage dependence of admittance characteristics of Al/Al_2O_3/PVA: n-ZnSe Schottky barrier diodes. Mater. Sci. Semicond. Process. **1**(41), 155–161 (2016)
6. A. Barkhordari, Ş Altındal, G. Pirgholi-Givi, H. Mashayekhi, S. Özçelik, Y. Azizian-Kalandaragh, The influence of PVC and (PVC: SnS) interfacial polymer layers on the electric and dielectric properties of Au/n-Si structure. SILICON **15**(2), 855–865 (2023)
7. Ş Altındal, A. Barkhordari, Y. Azizian-Kalandaragh, B.S. Çevrimli, H.R. Mashayekhi, Dielectric properties and negative-capacitance/dielectric in Au/n-Si structures with PVC and (PVC: Sm_2O_3) interlayer. Mater. Sci. Semicond. Process. **15**(147), 106754 (2022)
8. A. Azarov, A. Hallén, H.H. Radamson, Electrical characterization of semiconductors: I-V, C–V and hall measurements, in *Analytical methods and instruments for micro- and nanomaterials*. (Springer International Publishing, Cham, 2023), pp.197–240
9. B. Xu, G. Wang, Y. Du, Y. Miao, B. Li, X. Zhao, H. Lin, J. Yu, J. Su, Y. Dong, T. Ye, Monolithic integration of O-band InAs quantum dot lasers with engineered GaAs virtual substrate based on silicon. Nanomaterials **12**(15), 2704 (2022)
10. Y. Miao, H. Lin, B. Li, T. Dong, C. He, J. Du, X. Zhao, Z. Zhou, J. Su, H. Wang, Y. Dong, Review of Ge (GeSn) and InGaAs avalanche diodes operating in the SWIR spectral region. Nanomaterials **13**(3), 606 (2023)
11. J. Yu, X. Zhao, Y. Miao, J. Su, Z. Kong, H. Li, Y. Wu, Z. Zhou, B. Wang, T. Ye, H.H. Radamson, High-performance Ge PIN photodiodes on a 200 mm insulator with a resonant cavity structure and monolayer graphene absorber for SWIR detection. ACS Appl. Nano Mater. **7**(6), 5889–5898 (2024)
12. A.A. Alarabi, O. Çiçek, H. Makara, F. Ünal, M. Zurnacı, Ş Altındal, Enhanced sensing capabilities of UV–Visible pn and pin photodiodes using unique layer and contact configurations. Eng. Sci. Technol. Int. J. **1**(62), 101975 (2025)
13. L.E. Byrum, G. Ariyawansa, R.C. Jayasinghe, N. Dietz, A.G. Perera, S.G. Matsik, I.T. Ferguson, A. Bezinger, H.C. Liu, Negative capacitance in GaN/ AlGaN heterojunction dual-band detectors. J. Appl. Phys. **106**(5), 053701 (2009)
14. M. Ershov, H.C. Liu, L. Li, M. Buchanan, Z.R. Wasilewski, A.K. Jonscher, Negative capacitance effect in semiconductor devices. IEEE Trans. Electron Devices **45**(10), 2196–2206 (1998)
15. R. Gharbi, M. Abdelkrim, M. Fathallah, E. Tresso, S. Ferrero, C.F. Pirri, T.M. Brahim, Observation of negative capacitance in a-SiC: H/a-Si: H UV photodetectors. Solid-State Electron. **50**(3), 367–371 (2006)
16. J. Bisquert, G. Garcia-Belmonte, Á. Pitarch, H.J. Bolink, Negative capacitance caused by electron injection through interfacial states in organic light-emitting diodes. Chem. Phys. Lett. **422**(1–3), 184–191 (2006)
17. M.A. Alam, M. Si, P.D. Ye, A critical review of recent progress on negative capacitance field-effect transistors. Appl. Phys. Lett. **114**(9), 090401 (2019)
18. X. Wu, E.S. Yang, H.L. Evans, Negative capacitance at metal-semiconductor interfaces. J. Appl. Phys. **68**(6), 2845–2848 (1990)
19. M. Hoffmann, S. Slesazeck, T. Mikolajick, Progress and future prospects of negative capacitance electronics: A materials perspective. APL Mater. **9**(2), 020902 (2021)
20. S. Demirezen, E.E. Tanrıkulu, Ş Altındal, The study on negative dielectric properties of Al/PVA (Zn-doped)/p-Si (MPS) capacitors. Indian J. Phys. **4**(93), 739–747 (2019)
21. Y. Azizian-Kalandaragh, S. Özçelik, A. Barkhordari, Ş Altındal, A strategy to predict the current conduction mechanisms into Al/PVP: Gr-BaTiO3/p-Si Schottky structure using artificial neural network. Micro Nanostruct. **20**, 207957 (2024)
22. K.S. Butcher, T.L. Tansley, D. Alexiev, An instrumental solution to the phenomenon of negative capacitances in semiconductors. Solid-State Electron. **39**(3), 333–336 (1996)
23. X.L. Huang, Y.G. Shin, K.Y. Lim, E.K. Suh, H.J. Lee, S.C. Shen, Thermally induced capacitance and electric field domains in GaAsAl0.3Ga0.7As quantum well infrared photodetector. Solid-State Electron. **41**(6), 845–850 (1997)
24. C.Y. Zhu, L.F. Feng, C.D. Wang, H.X. Cong, G.Y. Zhang, Z.J. Yang, Z.Z. Chen, Negative capacitance in light-emitting devices. Solid-State Electron. **53**(3), 324–328 (2009)
25. R. Ertugrul-Uyar, A. Buyukbas-Ulusan, A.D. Tataroglu, Ionizing radiation effects on Au/TiO 2/n-Si metal–insulator-semiconductor (MIS) structure. J. Mater. Sci. Mater. Electron. **31**, 19846–19851 (2020)
26. R. Bjornsson, F. Neese, R.R. Schrock, O. Einsle, S. DeBeer, The discovery of Mo (III) in FeMoco: reuniting enzyme and model chemistry. J. Biol. Inorg. Chem. **20**, 447–460 (2015)
27. T. Prohaska, J. Irrgeher, J. Benefield, J.K. Böhlke, L.A. Chesson, T.B. Coplen, T. Ding, P.J. Dunn, M. Gröning, N.E. Holden, H.A. Meijer, Standard atomic weights of

the elements 2021 (IUPAC Technical Report). Pure Appl. Chem. **94**(5), 573–600 (2022)
28. I. Kajan, S. Heinitz, K. Kossert, P. Sprung, R. Dressler, D. Schumann, First direct determination of the 93Mo half-life. Sci. Rep. **11**(1), 19788 (2021)
29. S. Leimkühler, The biosynthesis of the molybdenum cofactors in Escherichia coli. Environ. Microbiol. **22**(6), 2007–2026 (2020)
30. Adout A, Hawlena D, Maman R, Paz-Tal O, Karpas Z, Albert L, Azimi S, Ludwig A, Thévenot DR, Colin JL, Bauman G. Considine, Glenn D. ed. 2005. Molybdenum. Van Nostrand's Encyclopedia of Chemistry.
31. Gupta CK. Extractive metallurgy of molybdenum. Routledge; 2017 Nov 13.
32. Z. Yang, K. Hu, D. Hu, C. Han, Y. Tong, X. Yang, F. Wei, J. Zhang, Y. Shen, J. Chen, X. Wu, Diffusion bonding between TZM alloy and WRe alloy by spark plasma sintering. J. Alloy. Compd. **5**(764), 582–590 (2018)
33. A. Barkhordari, S. Özçelik, Ş Altındal, G. Pirgholi-Givi, H. Mashayekhi, Y. Azizian-Kalandaragh, The effect of PVP: BaTiO3 interlayer on the conduction mechanism and electrical properties at MPS structures. Phys. Scr. **96**(8), 085805 (2021)
34. S.K. Cheung, N.W. Cheung, Extraction of Schottky diode parameters from forward current-voltage characteristics. Appl. Phys. Lett. **49**(2), 85–87 (1986)
35. H. Norde, A modified forward I-V plot for Schottky diodes with high series resistance. J. Appl. Phys. **50**(7), 5052–5053 (1979)
36. V.R. Reddy, Electrical properties of Au/polyvinylidene fluoride/n-InP Schottky diode with polymer interlayer. Thin Solid Films **1**(556), 300–306 (2014)
37. Ş Altındal, A. Barkhordari, S. Özçelik, G. Pirgholi-Givi, H.R. Mashayekhi, Y. Azizian-Kalandaragh, A comparison of electrical characteristics of Au/n-Si (MS) structures with PVC and (PVC: Sm2O3) polymer interlayer. Phys. Scr. **96**(12), 125838 (2021)
38. A. Buyukbas-Uluşan, S.A. Yerişkin, A.D. Tataroğlu, M. Balbaşı, Y.A. Kalandaragh, Electrical and impedance properties of MPS structure based on (Cu 2 O-CuO–PVA) interfacial layer. J. Mater. Sci. Mater. Electron. **29**, 8234–8243 (2018)
39. H. Schroeder, Poole-Frenkel-effect as dominating current mechanism in thin oxide films—An illusion?! J. Appl. Phys. **117**(21), 215103 (2015)
40. E. Marıl, A. Kaya, S. Koçyiğit, Ş Altındal, On the analysis of the leakage current in Au/Ca3Co4Ga0.001Ox/n-Si structure in the temperature range of 80–340 K. Mater. Sci. Semicond. Process. **31**, 256–261 (2015)
41. Schroder DK. Semiconductor material and device characterization. John Wiley & Sons; 2015 Jun 29.
42. D. Seghier, H.P. Gislason, Electrical characterization of Mg-related energy levels and the compensation mechanism in GaN: Mg. J. Appl. Phys. **88**(11), 6483–6487 (2000)
43. A. Barkhordari, S. Özçelik, G. Pirgholi-Givi, H.R. Mashayekhi, Ş Altındal, Y. Azizian-Kalandaragh, Dielectric properties of PVP: $BaTiO_3$ interlayer in the Al/PVP: BaTiO3/P-Si structure. SILICON **14**(10), 5437–5443 (2022)
44. F.B. Abdallah, A. Benali, M. Triki, E. Dhahri, M.P. Graca, M.A. Valente, Effect of annealing temperature on structural, morphology and dielectric properties of La0.75Ba0.25FeO3 perovskite. Superlattices Microstruct. **117**, 260–270 (2018)
45. O. Çiçek, H.U. Tecimer, S.O. Tan, H. Tecimer, Ş Altındal, I. Uslu, Evaluation of electrical and photovoltaic behaviours as comparative of Au/n-GaAs (MS) diodes with and without pure and graphene (Gr)-doped polyvinyl alcohol (PVA) interfacial layer under dark and illuminated conditions. Compos. B Eng. **1**(98), 260–268 (2016)
46. O.G. Abdullah, Y.A. Salman, S.A. Saleem, Electrical conductivity and dielectric characteristics of in situ prepared PVA/HgS nanocomposite films. J. Mater. Sci. Mater. Electron. **27**, 3591–3598 (2016)
47. Ş Altındal, A. Barkhordari, G. Pirgholi-Givi, M. Ulusoy, H. Mashayekhi, S. Özçelik, Y. Azizian-Kalandaragh, Comparison of the electrical and impedance properties of Au/(ZnOMn: PVP)/n-Si (MPS) type Schottky-diodes (SDs) before and after gamma-irradiation. Phys. Scr. **96**(12), 125881 (2021)
48. G. Bator, Ac and dc conductivity around the ferroelectric phase transition in (CH3NH3) 3Bi2Br 9 (MABB) crystal. Ferroelectrics **200**(1), 287–295 (1997)
49. H.N. Chandrakala, B. Ramaraj, Shivakumaraiah, G.M. Madhu, F. Siddaramaiah, The influence of zinc oxide–cerium oxide nanoparticles on the structural characteristics and electrical properties of polyvinyl alcohol films. J. Mater. Sci. **47**, 8076–8084 (2012)
50. N. Delen, S.A. Yerişkin, A.K. Özbay, İ Taşçıoğlu, Origin of frequency and voltage dependent negative dielectric properties in the Al/p-Si Schottky diodes with (Cd0.3Zn0.7O) interfacial layer in the wide range of frequency and voltage. Physica B **665**, 415031 (2023)
51. Ç.Ş Güçlü, S.A. Hameed, A. Khalkhali, İ Taşçıoğlu, Ş Altındal, A detailed analysis of electrical parameters and energy dependence of interface Traps in Au-(Co: PVA)-nSi-Al structure via impedance measurements. J. Mater. Sci. Mater. Electron. **36**(14), 1–3 (2025)

52. A. Turut, H. Efeoğlu, Numerical Analysis of Thermal Sensitivity Characteristics by Pinch-Off Model in Inhomogeneous Schottky Barrier Diodes. J. Electron. Mater. **20**, 1–1 (2025)