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Electrical and dielectric behaviors of Al/SiO_2-surfactant/n-Si schottky structure in wide range of voltage and frequency

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Abstract

SiO_2 surfactant insulator into Al/n-Si metal-semiconductor (MS) structure was fabricated into Al/SiO_2-surfactant/n-Si metal–insulator–semiconductor (MIS) structure and its effect on the electrical properties of the final structure was investigated. The SiO_2-surfactant layer is coated on the n-Si wafer by the spin coating technique. The I-V data is used to calculate the fundamental electrical parameters of this MIS structure. The density distribution of the surface states (N_{ss}) is computed depending on the energy at forward potential. The current conduction mechanisms (CCMs) in the MIS structure are examined at the reverse and forward biases applied. To get more accurate and reliable results, the profiles of I-V and C/(G/ω)-V are measured at a wide range of bias voltage (0.25V-4V) and frequency (1kHz-1MHz), respectively. The performance of the MIS is significant due to the basic values of electrical parameters (n, I_0, R_s, R_{sh}, N_{ss}, Φ_{B0}, and Rectifying Ration (RR)) and dielectric parameters (ε', ε'', tan δ, M′, M″, R_s, and σ) compared with the MS structure. The other electrical parameters (N_D, W_D, E_m, Φ_B) are extracted from the slope and intercept of the reverse bias C^{-2}-V plot as a function of frequency. Furthermore, the profile of voltage-dependent R_s and N_{ss} was determined using different methods from I-V and C/G-V data and examined comparatively with each other. The changes in impedance properties with frequency and voltage of the MIS are discussed in detail.

1. Introduction

The Metal/Semiconductor (MS) configurations are essential for the optimal performance of some landmark electronic devices such as transistors, photo-diodes (PDs), Schottky diodes (SDs), solar cells (SCs) that, without them, would not be able to function at their full potential [1, 2]. Due to their versatility, they can be used for both rectifying and non-rectifying purposes. Recently, the design of metal-insulator/polymer-semiconductor (MIS/MPS) structures has become increasingly fascinating as a means of controlling and raising the potential barrier height (BH) and improving the electric and dielectric efficiency of the MS structures [3]. These structures are made when an oxide or insulator layer is present at the interface of the metal and semiconductor layers. As a suitable alternative to the MS structure in electronic and optoelectronic devices, these MIS/MPS structures enhance the performance of an MS diode by changing the most influential factors, such as series resistance (R_s), barrier inhomogeneity and interface traps/states (N_{it}, N_{ss}) [4]. In addition to varying the electric properties of the MS structure due to the presence of an interfacial layer at the M/S interface, the capacitance (C) and conductance (G/ω) of the MIS/MPS device are significantly altered in response to changes in voltage and

frequency, originating from the variation of the N_{ss} distribution at the interlayer/semiconductor interface as well as the R_s. At lower frequencies, polarization processes and surface states are more efficient in the depletion region, whereas the interfacial layer and R_s are more efficient in the accumulation region at higher frequencies [5]. So, these structures' electric and dielectric performance depends on the N_{ss} distribution, R_s, material, thickness, homogeneity, and permittivity of the interlayer used.

It is worth mentioning that silicon (Si) is a widely-occurring element in nature, and is most commonly used in semiconductor technology. One of the key features of Si is its ability to form an oxide layer ($Si+O_2 = SiO_2$) known as an insulator. SiO_2 is also a very stable, highly reproducible metal-oxide material that can be easily grown on semiconductors both native and deposited by various methods such as thermal or wet oxidation and sputtering. The fabrication of MIS-type SDs relies heavily on the deposition of the oxide or insulator on the semiconductor device surface, which can significantly affect the stability and reliability of the device [1]. The expansion of application areas in optoelectronics and high-frequency applications has led to increased interest in these devices recently. MIS-type SDs have a thin insulation layer at the M/S interface. This interface layer provides an effective solution to prevent the diffusion between the semiconductor layer and the metal and the resulting electric field reduction problem in MIS-type SDs [6]. In MIS type SD, an insulating layer located between the metal and semiconductor layers gives the device a capacitor feature, allowing it to store electrical charges or energy due to the dielectric structure of the oxide layers. Traditional techniques used to passivate the active bonds on the surface of the Si semiconductor and to create an insulating layer on this semiconductor are insufficient. Also, it should be mentioned that oxygen ions create space charge effects at low frequencies that can be quite pronounced [7]. The effectiveness and dependability of these MIS devices are largely determined by the presence of the interfacial insulator layer between the Si and SiO_2 layers. Also, the interface states distribution has an important role in the effectiveness of the MIS devices. Recently, owing to the technical significance of the MIS-type SDs, there has been a surge of research in the literature [8–12]. Despite this, a comprehensive study on voltage- and frequency-dependent electric and dielectric characteristics of the MS-type SD with a SiO_2 insulator interfacial layer remains largely unexplored.

In this work, the goal is to analyze the electronic and dielectric specifications of the MS-type SD with a SiO_2-surfactant insulator at the M/S interface for potential use in electronic applications, focusing on the I-V, C/(G/ω)-V, and C/(G/ω)-f characteristics. To this, an MIS-type SD with a structure of Al/SiO_2-surfactant /n-Si is created on the Si wafer under a condition that is thoroughly described in the next section. After measuring the I-V characteristics from −4.5 V to 4.5 V and by employing TE, Norde, and Cheung functions, the primary electronic variables of the presented structure including I_0, n, BH, R_{sh}, and R_s, are calculated and compared. Next, the Card-Rhoderick method is applied to extract the energy-dependent profile of N_{ss} at the forward-bias region. The current conduction mechanisms (CCMs) in the Al/SiO_2-surfactant/n-Si MIS-type SD are determined at the forward-bias voltages and reverse-bias voltages. Then, the voltage- and frequency-dependent impedance (C/(G/ω)-V, C/(G/ω)-f) of the structure is measured at a voltage range from 0.25 V to 4 V and a frequency range of 1kHz-1MHz to extract the ε', ε'', tan δ, R_s, and σ of the structure. The C^{-2}-V profile of the structure is also studied at the frequency of 1kHz-1MHz. Finally, the obtained experimental findings are explained in detail.

2. Materials and experiment

2.1. Synthesis of SiO_2-surfactant sol–gel insulator

2.1.1. The sol–gel solution was prepared as follows

The silica source Tetraethyl orthosilicate (TEOS) was mixed with Ethanol, H_2O, and HCl 37%; 0.56 g of the surfactant (Brij58) was dissolved in Ethanol. The two solutions were stirred at room temperature for 1 h, then mixed and stirred for 1 h before spin coating. The final molar ratio solution (TEOS: B rij58:H_2O:EtOH: HCl) was 1:0.05:5.2:24:0.28 [13, 14]. The mesoporous material precursor solution was then spin-coated on the n-Si wafer at 2000 rpm for 1 min. The resulting sol–gel is composed of surfactant tubular micelles surrounded by silica precursor in a cubic order. The surfactant tubes have a diameter of 3–4 nm.

It is necessary to mention that a single crystal n-Si wafer (380 μm thicknesses), 2-inch diameter, and a resistance of 1–10 $\Omega.cm^{-1}$ was used as the substrate for the Al/SiO_2-surfactant structure. A thermal evaporation technique (coating pressure 10^{-6} Torr) was employed to coat the underside of the wafer with an Al layer of 150 nm thickness. Then the sample was annealed at 500 °C in a Rapid Thermal Annealing (RTA) system to make an ohmic contact. At the last step, an Al/SiO_2-surfactant/n-Si MIS type SD structure was realized by making 150 nm thick Al Schottky contacts on the surfactant insulator layer using 1.2 mm diameter dot masks.

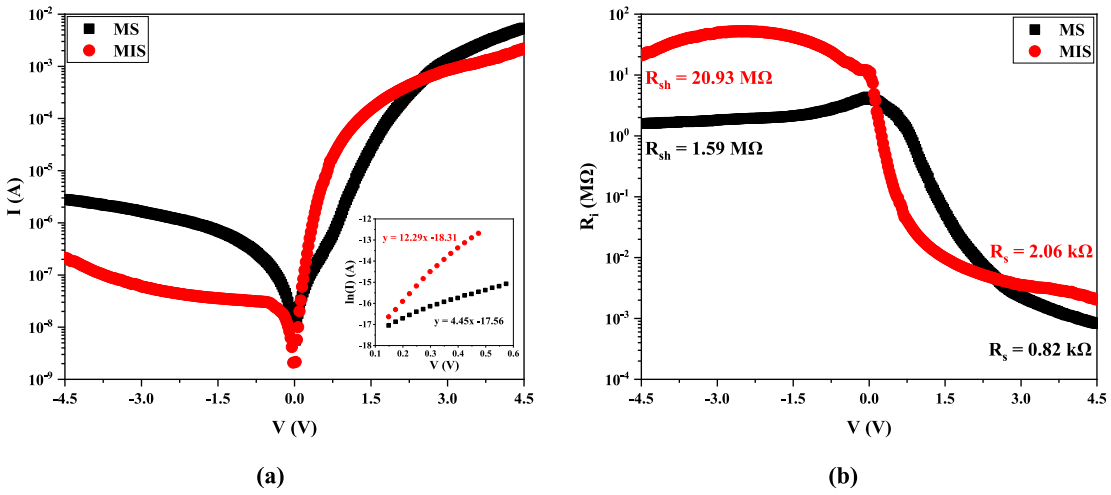

Figure 1. The semi-logarithmic profiles of (a) I-V and (b) R_i-V for the MS and MIS structures.

3. Results and discussion

3.1. Current–voltage (I-V) characteristics

3.1.1. Thermionic Emission (TE) theory

The transfer of electrons and holes with enough thermal energy to overcome the BH is known as the Thermionic Emission (TE) theory [15]. This theory is used to determine the fundamental electronic variables of the MS configurations without/with an interlayer at the M/S interface, based on the current–voltage (I-V) data in the forward bias region. However, because of R_s, D_{it}, interlayer, and the inhomogeneity of the potential barrier formed at the junction, the ideal case of the I-V relationship in the MS/MIS configurations possessing series resistance with n>1 and V⩾3kT/q is sometimes not observed (see figure 1(a)). Based on TE theory, the relationship of I-V in these configurations is expressed as [16]:

$$I = \underbrace{AA^{*}T^{2}\exp\left(-\frac{q}{kT}\Phi_{B0}\right)}_{I_0}\left[\exp\left(\frac{q(\mathrm{v}-IR_s)}{nkT}\right)-1\right] \tag{1}$$

Here, n refers to the ideality factor, Φ_{B0} denotes the potential BH, I_0 and A^* are the reverse-saturation current and the Richardson-constant, respectively. The other parameters are well-introduced in the literature [15–17]. The value of I_0 is determined by the intercept of ln(I)-V profile at 0 V (see the inset of figure 1(a)), and then using rectifier-contact area, the Φ_{B0} can be obtained as follows [2, 17]:

$$\Phi_{B0} = \frac{kT}{q}Ln\left(\frac{AA^{*}T^{2}}{I_0}\right) \tag{2}$$

The values of I_0 and Φ_{B0} are calculated to be 2.27×10^{-8} A and 0.78 eV for the MS structure, 1.13×10^{-8} A and 0.80 eV for the MIS structure. The value of n is a measure of the quality of MS/MIS-type SDs, and ideally, it should be equal to 1. However, in practical applications, the value of n found out by the slope of the ln(I)-V profile is usually greater than 1, due to the thickness of interlayer (δ_i), depletion layer width (W_D), interface-traps (D_{it}), and dielectric value (ε_i) of interlayer as given by [2, 18]:

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln(I))}\right) = 1+\left(\frac{\delta_i}{\varepsilon_i}\right)\left\{\frac{\varepsilon_s}{W_D}+qD_{it}\right\} \tag{3}$$

The n value of the MS and MIS structures was respectively obtained to be 8.59 and 3.14 which is greater than unity due to the above explanations and barrier inhomogeneity. The resistance of the MIS structure can be computed as a function of voltages by Ohm's law ($R_j = dV_j/dI_j$) [19]. At a forward voltage of 4.5 V, the resistance corresponded to the series resistance (R_s), while at a low reverse voltage, it corresponded to shunt resistance (R_{sh}) as observed in figure 1(b). The values of R_s and R_{sh} for the MS and MIS structures are 0.82 kΩ and 1.59 MΩ for the MS structure, 2.06 kΩ and 20.93 MΩ for the MIS structure, respectively. Moreover, the rectifier ratio ($RR = I_F/I_R$) is a key factor in determining the performance of MS and MIS structures that equals 1.93×10^{3} and 10.15×10^{3}, respectively, which indicates that the SD has good rectifier behavior.

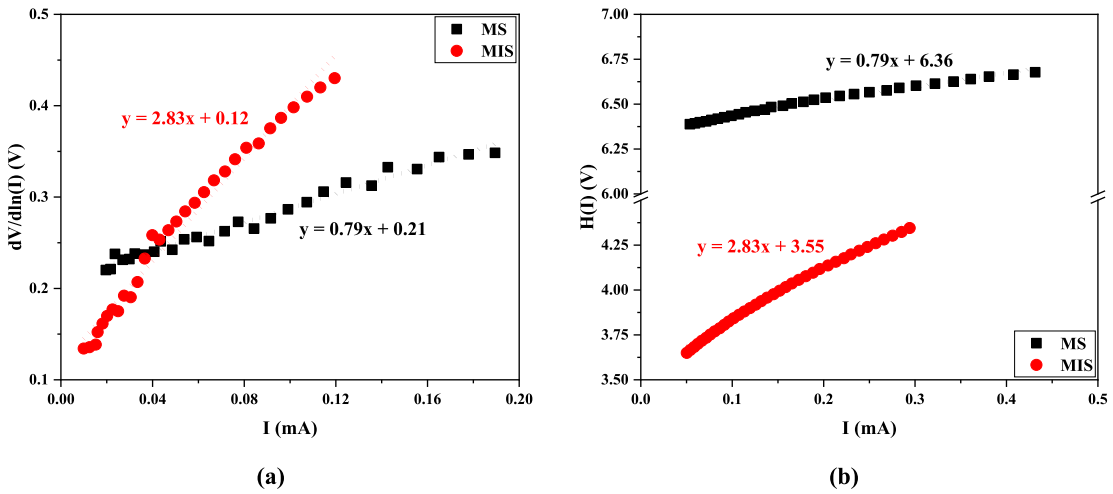

Figure 2. The profiles of (a) dV/d(ln(I)) and (b) H(I) of the MS and MIS samples.

Table 1. Electronic factors of the MS and MIS samples computed by I-V measurement.

Diode	Φ_{B0} (eV)			RR × 10^3	R_s (kΩ)				R_{sh} (MΩ)	n		$N_{ss} \times 10^{13}$ ($eV^{-1}.cm^{-2}$)	
	TE	Norde	H(I)		TE	Norde	H(I)	dV/dln(I)		TE	dV/dln(I)	TE	Norde
MS	0.78	0.83	0.79	1.93	0.82	0.81	0.79	0.79	1.59	8.59	8.08	4.18	3.51
MIS	0.80	0.81	0.80	10.15	2.06	3.02	2.83	2.83	20.93	3.14	4.50	0.32	0.49

3.1.2. Cheung functions

The second method for calculating the main electrical parameters of the MS and MIS structures such as n, Φ_{B0}, and R_s is to utilize the Cheung functions at the high forward bias voltage region, which corresponds to the concave-curvature of ln(I)-V profiles, through the use of the following two-relations [20, 21]:

$$\frac{dV}{d(\ln(I))} = IR_s + \left(\frac{nkT}{q}\right) \tag{4}$$

$$H(I) = V - \frac{nkT}{q}\ln\left(\frac{I}{AA^*T^2}\right) = IR_s + n\Phi_{B0} \tag{5}$$

Generally, the linearity behavior of the ln(I)-V profile loses at the forward bias voltage region, originating from the influences of R_s and the native or deposited interlayer. Cheung functions provide a linear section in this region, allowing R_s and n amounts to be computed by the slope and intercept of dV/d(ln(I))-I profile using equation (4). Additionally, the second-Φ_{B0} and R_s values can be determined from the slope and intercept of H(I)-I plot using equation (5). Using the slopes and intercepts introduced in figure 2, the values of n, Φ_{B0}, and R_s were computed and represented in table 1.

3.1.3. Norde method

It can be found out the values of R_s and BH for the MS and MIS structures with the Norde function, F(V). This function is expressed as [21]:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\left[Ln\left(\frac{I(V)}{AA^*T^2}\right)\right] \tag{6}$$

with γ being an integer greater than n. The voltage-dependent variations of F(V) for the MS and MIS structures are illustrated in figure 3(a). As seen, there is a minimum base point at the concave region of F(V) function, allowing R_s and Φ_{B0} to be computed by the Norde function [21] represented in table 1. The observed some discrepancies in the value of n, Φ_{B0}, and R_s obtained TE theory, Cheung and Norde functions are the result of voltage-dependent values of them or calculation method which are corresponding to different voltage and current range.

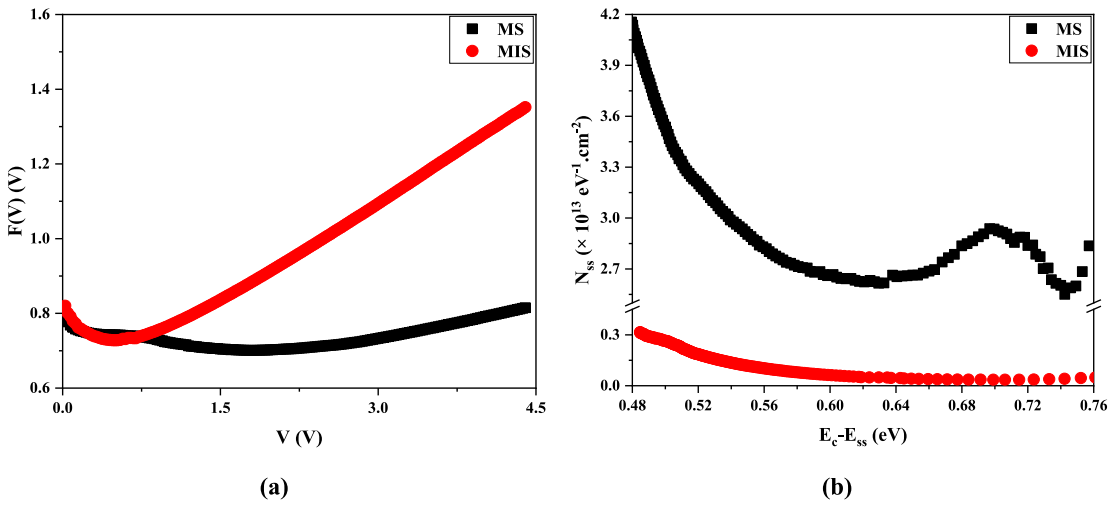

Figure 3. The function of (a) F(V) versus voltage and (b) N_{ss} versus energy for the MS and MIS samples.

Moreover, the interface states/trap density (N_{ss}) is a key factor that influences the non-ideal behavior of the MS and MIS structures. The I-V data at the forward bias voltage can be used to determine the N_{ss} profile in terms of energy by taking cognizance of the n(V) and Φ_{B0}(V). The interface states (N_{ss}) density at an equilibrium condition could be described as [2, 15]:

$$qN_{ss}(V) = \varepsilon_0 \left[\frac{\varepsilon_i}{d_i}(n(V) - 1) - \frac{\varepsilon_s}{W_D} \right] \tag{7}$$

Here, the permittivity of vacuum ε_0, is equal to 8.85×10^{-14} F/cm for free space or vacuum, the interlayer thickness, d_i, is equal to 200 nm examined by SEM image cross-section, and the width of the depletion layer, W_D, is 0.24 μm obtained from the intercept point of reverse bias C^{-2} versus V plot at 1 MHz. Furthermore, the factors of ε_s and ε_i correspond to the dielectric constant, respectively. The energy gap between the conduction band edge (E_c) and the N_{ss} level (E_{ss}) of an n-type semiconductor can be expressed as $E_c - E_{ss} = q(\varphi_e - V)$ [2, 16]. Variations of the energy-dependent graph of N_{ss} for the MS and MIS structures are presented in figure 3(b). The highest amount of N_{ss} for the MS and MIS structures is observed at 0.48 eV which are 4.18×10^{13} $eV^{-1}.cm^{-2}$ and 0.32×10^{13} $eV^{-1}.cm^{-2}$. Then its value gradually decreases with the increase of energy and finally reaches the smallest value at 0.74 eV. Generally, the value of N_{ss} for the MIS structure is significantly lower than that of the MS structure, originating from presenting an insulator interlayer at the M/S interface, resulting in semiconductor surface passivation [2, 22].

The primary electronic factors of MIS structure that have been computed by TE theory, Norde, and Cheung procedures are briefly represented in table 1. As can be seen, the results obtained by different methods for each parameter are in good agreement with each other. Inserting the SiO_2 insulator layer between the semiconductor and metal results in increasing the potential BH, R_{sh}, and RR and reducing the ideality factor and interface state density. However, the SiO_2 insulator layer leads to a relatively rising series resistance compared to the MS structure.

3.2. Current transport/conduction mechanisms (CTMs/CCMs)

The impact of the SiO_2-surfactant interlayer on the CCMs of the MS structure has been investigated under both forward and reverse bias conditions. The graph of $\ln(I_F)$ as a function of $\ln(V_F)$ for the MS and MIS structures is illustrated in figure 4(a), including three parts with different slopes due to different CCMs. From a general point of view, the charge transport is significantly improved when deep traps are created at the M/S interface. The profile of the MS and MIS structures consists of three linear parts with slope values of 1.23, 5.86, 3.44, and 1.62, 3.62, and 2.52, respectively. At the first region, the observed behavior is ohmic (I~V), with a relatively small bias voltage. This results in a close slope to unity, and a low amount of electric charge being syringed into the semiconductor from the electrodes [23]. In the secondary and third parts of this graph when the slope is greater than two, the electric current is exponentially changed ($I \sim \exp(cV)$) due to the dominance of recombination-tunneling as the primary charge carrier mechanism [24].

Both mechanisms of Poole–Frenkel (PF) and Schottky emissions (SE) are able to be used for studying the CCMs in the MIS structure. If the PFE process is predominant, the I_R would be [24, 25],

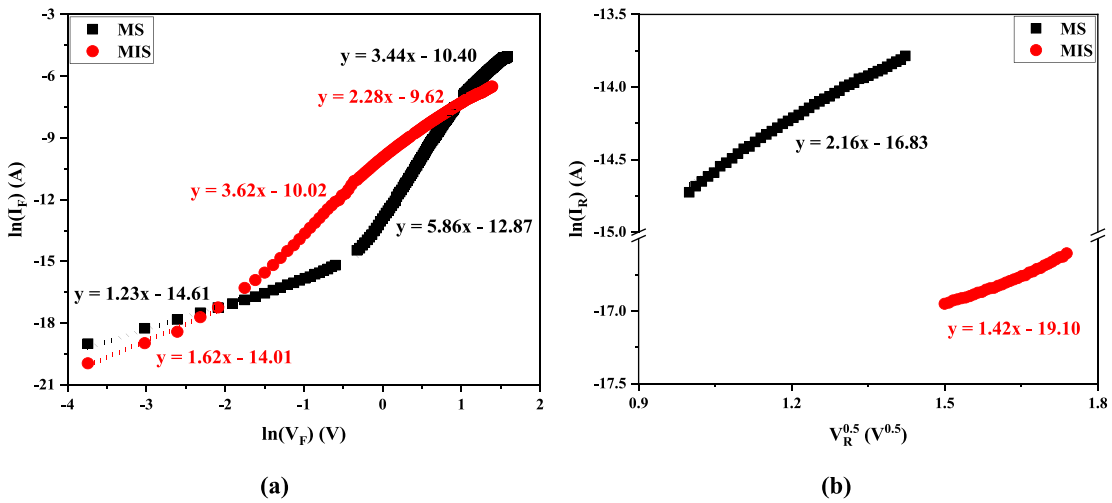

Figure 4. The (a) $\ln(I_F)$-V_F and (b) $\ln(I_R)$-$V_R^{0.5}$ graphs for the MS and MIS samples.

$$I_R = I_0 \exp\left(\frac{\beta_{PF}}{kT}\sqrt{\frac{V}{d}}\right) \tag{8}$$

Whereas the I_R is given by the following equation, with the condition that the SE mechanism is dominant,

$$I_R = AA^*T^2 \exp\left(-\frac{\varphi_B}{kT}\right)\exp\left(\frac{\beta_{SC}}{kT}\sqrt{\frac{V}{d_i}}\right) \tag{9}$$

where the factors of the field lowering for SE and PFE processes, i.e., β_{PF} and β_{SC}, are related to each other in the following way: $2\beta_{SC} = \beta_{PF}$ [25, 26].

The MS and MIS structures show the changes in $\ln(I_R)$-$V_R^{0.5}$ at room temperature in figure 4(b). The plot of the MS and MIS structures demonstrates a linear behavior. Consequently, the slope of these lines can be applied for computing the field lowering coefficient, which was determined to be $4.43 \times 10^{-6}\,eV^{-1}m^{0.5}V^{0.5}$ and $1.18 \times 10^{-5}\,eV^{-1}m^{0.5}V^{0.5}$ for the MS and MIS structures, respectively. The theoretical calculation of β_{PF} was equal to $3.79 \times 10^{-5}\,eV^{-1}m^{0.5}V^{0.5}$ for both MS and MIS structures. Therefore, the SE mechanism is the dominant CCM in the MS structure whereas the PFE process is the dominant CCM in the MIS structure by comparing the theoretical and experimental results.

3.3. Voltage-dependent Impedance (C/(G/ω)-V) of the sample

Figure 5 illustrates the C-V and G/ω-V profiles at a frequency range of 1 kHz to 1 MHz and room temperature for the MIS structure. Figure 5(a) reveals that the C-V and G/ω-V plots of the MIS structure exhibit inversion, depletion, and accumulation regions like the Metal-Oxide-Silicon (MOS) structure. In the depletion region, the C-V curve of the MIS structure has no peak, but they are raised and reduced by increasing the applied bias voltage and the frequency, respectively. The C-V curves of the MIS structure imply the passivation of active dangling bonds in the semiconductor crystalline due to an interfacial layer. The presence of un-passivated N_{ss} and bulk traps allow for the storage and release of numerous charges when a forward bias voltage is applied, resulting in an increase or decrease. Moreover, a distinctive peak is observed at the G/ω-V plots of MIS structure in figure 6(b), originating from a unique density distribution of N_{ss} and dislocation conditions between the semiconductor and interfacial layer at its forbidden energy bandgap [2, 27]. As seen in figure 5(a), the C-V profiles in the accumulation region display a concave curvature, resulting in the R_s and the interfacial layer. This implies that Nss is dominant in both depletion and inversion regions, while Rs and the interfacial layer are dominant only in the accumulation region.

The permittivity of SDs is a complex parameter ($\varepsilon^* = \varepsilon' - j\varepsilon''$) that plays a significant role in their dielectric properties. The stored energy of the structure is represented by

$$\varepsilon' = C/C_0 = Cd_i/\varepsilon_0 A, \tag{10}$$

while the loss energy is indicated by

$$\varepsilon'' = G/\omega C_0 = Gd_i/\varepsilon_0 \omega A, \tag{11}$$

with $C_0 = \varepsilon_0 A/d_i$ being the geometric capacitance, ε_0 the dielectric constant of free space, A the rectifier junction space, and d_i the thickness of the interlayer [28]. Figures 6(a) and (b) exhibit the changes of ε' and ε'' in

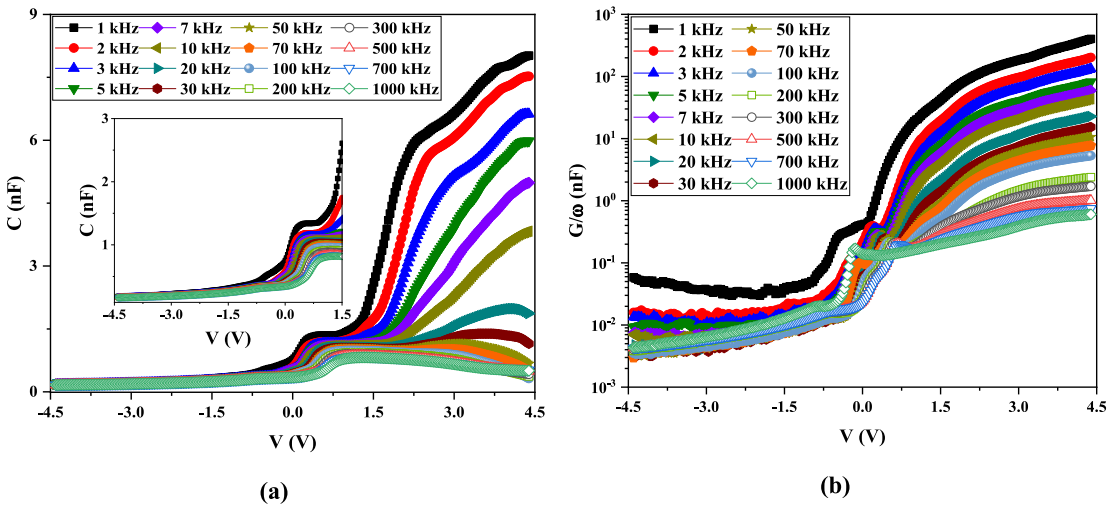

Figure 5. The variations of (a) C (b) G/ω versus V for the MIS sample.

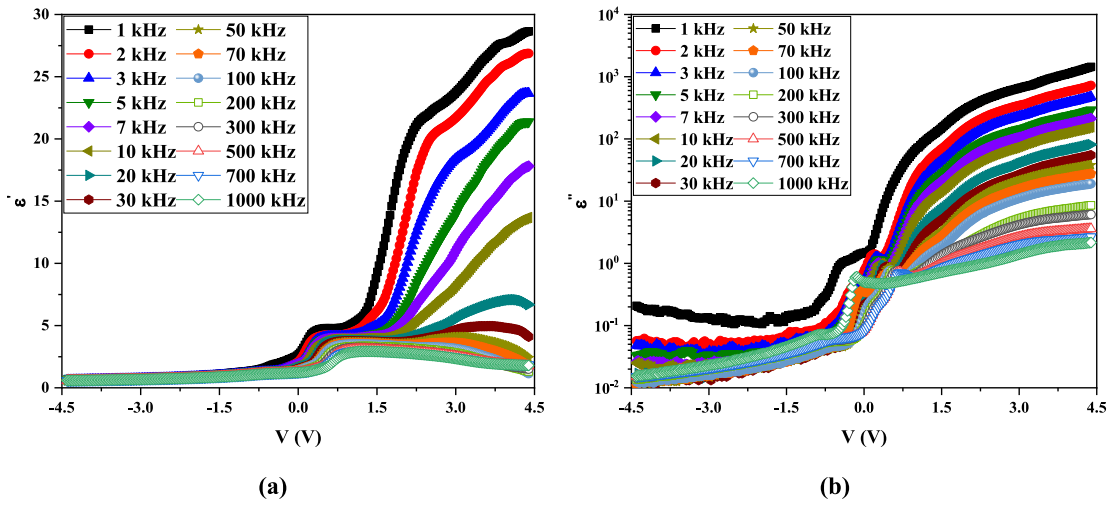

Figure 6. The function of (a) ε' and (b) ε'' versus V for the MIS sample.

terms of applied bias voltage for the MIS structure in the 1kHz-1MHz frequency range and room temperature. It can be observed that the parameters of ε' and ε'' strongly depend on the applied bias voltage and the frequency, particularly in the depletion and accumulation regions. With increasing frequency, the values of the parameters ε' and ε'' decrease in these regions, but remain constant in the inversion region. It must be noted that the R_s of this MIS structure is the main reason behind such behavior of ε' and ε'' functions [29]. Additionally, the dispersion observed in the ε' and ε'' functions with the frequency is related to the Maxwell–Wagner [30] and space-charge polarization [31].

Additionally, the electro-physical parameter known as tangent loss, tanδ, is defined as,

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} = \frac{G}{\omega C} \tag{12}$$

δ refers to the phase difference between the applied electric field and the induced current [28]. Figure 7(a) represents the voltage-dependent tanδ in the 1kHz-1MHz frequency range at room temperature. The values of tanδ for the MIS structure give a peak almost at all frequency regions. As frequency increases, the peak values of these measurements decrease and the peak positions move towards the negative-bias region. The peak value of tanδ is influenced by a variety of factors, including interface state density, series resistance, and the thickness of the interfacial insulator layer [32]. It is widely acknowledged that capacitance and conductance phenomena are susceptible to the interface characteristics, as the interface states react differently to low and high frequencies [33]. Previous studies have suggested that the peak observed is due to interlayer states [34–36].

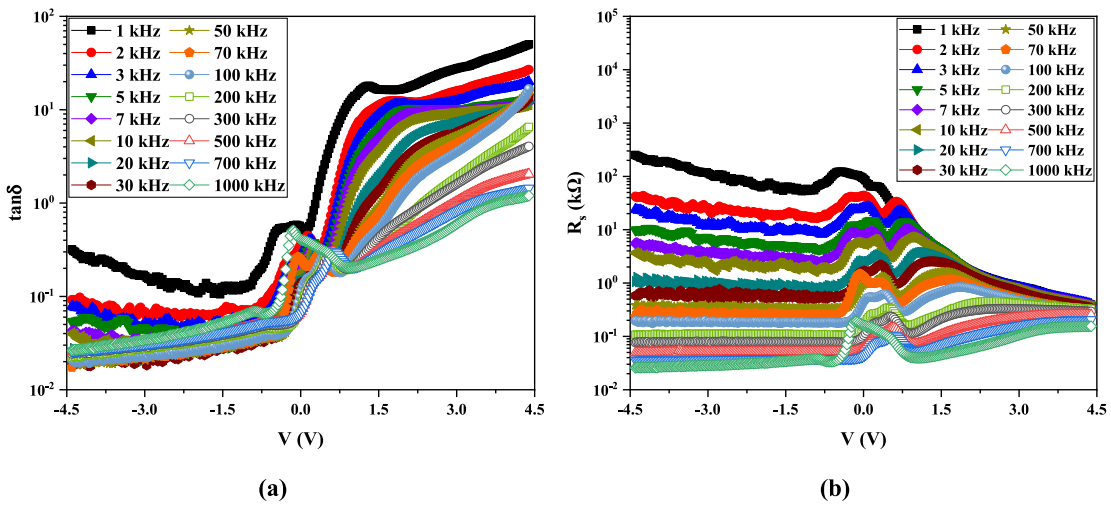

Figure 7. The changes of (a) tan δ and (b) R_s versus V for the MIS sample.

It is important to note that the series resistance, Rs, can be decreased by reducing the potential barrier height at the interface of M/S or using a highly doped semiconductor material. According to the Nicollian and Brews technique, the changes in the frequency-dependent series resistance can be expressed as follows [37]:

$$R_s = \frac{G}{G^2 + (\omega C)^2} \tag{13}$$

with C being the capacitance and G/ω conductance at the applied bias voltages. To confirm the impact of R_s on the C-V and G/ω-V characteristics, voltage-dependent profiles of R_s for the MIS structure are presented in figure 7(b). As shown, the value of Rs becomes nearly constant at a vital accumulation region, thus corresponding to the actual value of Rs for the MIS structure.

Furthermore, the profile of voltage-dependent R_s for the MIS structure reveals the impact of the density distribution of N_{ss} between the interfacial layer and the semiconductor, as well as their relaxation times, on the peak behavior at all frequencies. Restructuring and reordering of N_{ss} under applied bias voltage also play a role. In the inversion region of low frequencies, the effect of R_s is negligible, but it is more pronounced at high frequencies and in the accumulation region.

To survey the electric conduction processes and to specify the grains and grin boundary contributions by the elimination of the electrode polarization response in the MIS structures, the electrical modulus must be computed. It is a complex parameter ($M^* = M' - jM''$) whose real and imaginary parts are given by [38]:

$$M' = \omega C_0 Z'' = \varepsilon'/(\varepsilon'^2 + \varepsilon''^2) \tag{14a}$$

$$M'' = \omega C_0 Z' = \varepsilon\varepsilon''/(\varepsilon'^2 + \varepsilon''^2) \tag{14b}$$

Figure 8(a) shows the room temperature results of the evolution of M′ curves in the frequency range 1kHz-1 MHz at different voltage values. It is clear that the maximum values of M' in the entire frequency range are observed at the applied voltage of −4.5 V and after that, the M' values decrease with the increase of applied voltages and reach tear zero at +4.5 versus On the other hand, the M″ quantity is increased by increasing the frequency, originating from the monoatomic dispersion due to the short-range mobility of charge carriers. Additionally, the variation of the connected M″ profiles in the 1kHz-1MHz frequency range at different voltage values at room temperature is shown in figure 8(b). It can be seen that the values of M″ are almost constant at the applied voltages between −4.5 V and +4.5 versus In addition, a sharp peak appears near zero voltage. Contrary to the M' behavior, the M″ curves are reduced as the frequency increases.

Figure 9(a) presents the M″- M′ profiles of the fabricated MIS structure for the selected frequencies of 1 kHz, 10 kHz, 50 kHz, and 100 kHz. At these frequencies, a successive semicircular arc that indicates the polarization mechanism at the interlayer owing to the effects of grains instead of grin boundaries is observed and both grain and grain boundary contributions with their electric resistances can be distinguished. The Cole-Cole profiles are a single semicircle that can be modeled by an equivalent circuit together with the parallel capacitance (C_p) & and resistance (R_p) network in series with R_s [13, 39].

The depletion layer capacitance of the MIS SD structure can be calculated for the reverse region as follows [1, 2]:

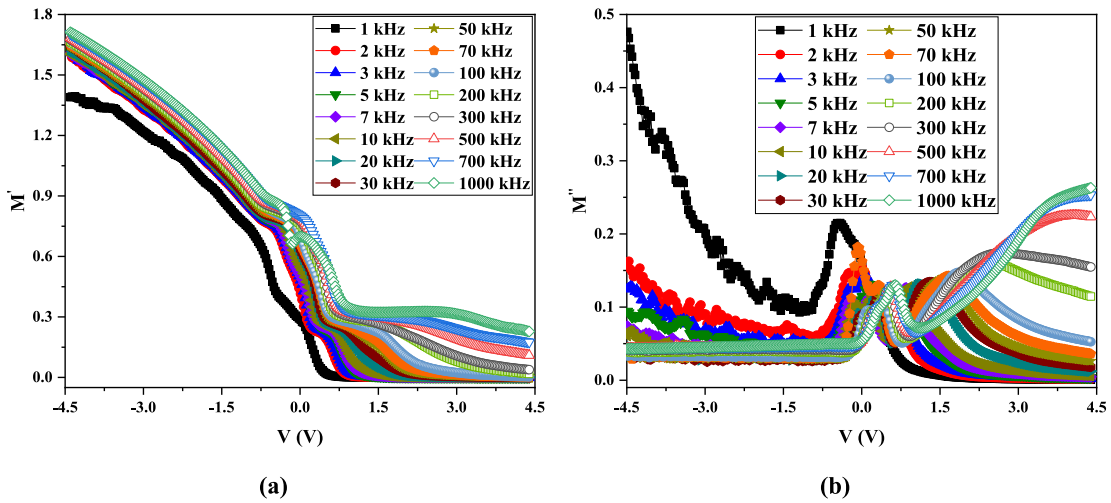

Figure 8. The plots of (a) M′ and (b) M″ versus V for the MIS sample.

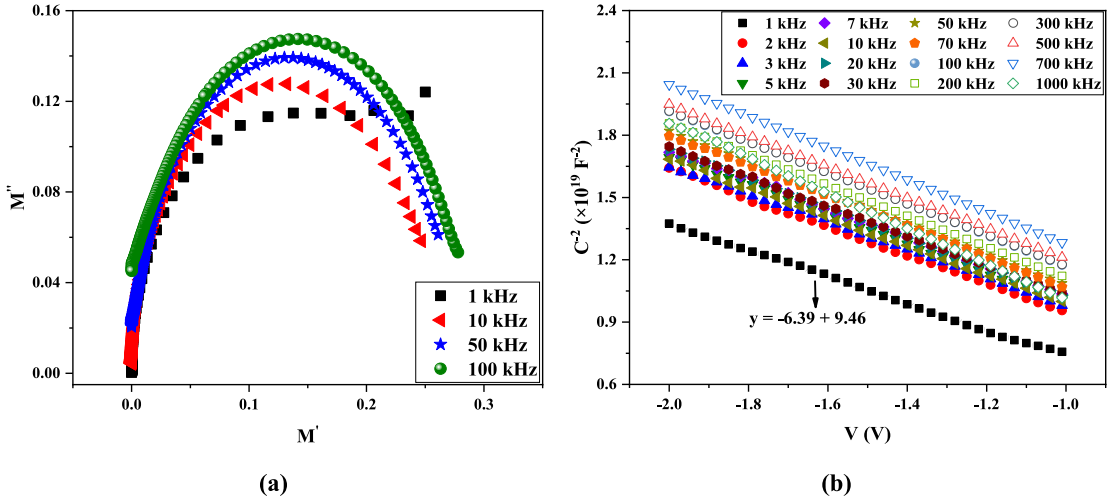

Figure 9. The plots of (a) M″-M′ and (b) C^{-2}-V profiles for the MIS sample.

$$C^{-2} = \frac{2(V_0 - kT/q + V_R)}{qA^2\varepsilon_0\varepsilon_s N_D} \tag{15}$$

Here, C denotes the measured capacitance, V refers to the applied bias voltage, q is the electronic charge, A is the MIS area, and ε_0 and ε_s are the permittivity of the vacuum and semiconductor [1, 2]. Moreover, N_D denotes the doping content of donor atoms and V_d is the non-biased diffusion potential determined by the intercept of the C^{-2}-V profile. The main electronic parameters of the MIS structure such as N_D, the width of the depletion layer (W_d), barrier height (Φ_B), and Fermi energy (E_F) in each applied frequency can be calculated by the C^{-2}-V profile. Figure 10(b) depicts the voltage-dependent C^{-2} profiles for the MIS-type SD at the different frequencies in the reverse bias region. As shown, the slope of C^{-2}-V plots for the MIS-type SD implies a good linear relation between C^{-2} and applied bias voltage from −2 V to −1 V, and it slightly increases by growing the frequency up.

The amount of intercept voltage (V_0) and N_D had been calculated by the usage of the intercept and slope of the C-V graph at each frequency. Furtherly, Fermi energy level and barrier height values are given for the MIS structure as follows [37],

$$E_F = \frac{kT}{q}\ln\left(\frac{N_C}{N_D}\right) \tag{16}$$

$$\Phi_B = V_0 + kT/q + E_F - \Delta\Phi_B \tag{17}$$

with kT/q being the thermal energy, N_c the states density at the conduction band, and $\Delta\Phi_B$ the image force lowering. On the other hand, the quantity of N_D and W_d can be computed by the slope (tan θ) and intercept

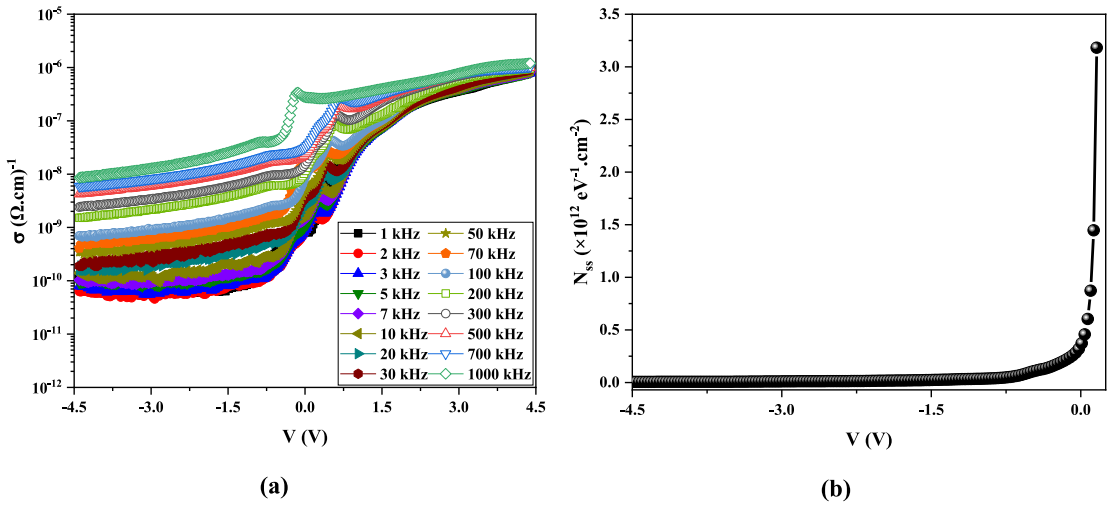

Figure 10. The plots of (a) σ and (b) N_{ss} versus V for the MIS sample.

Table 2. Electronic parameters of the MIS sample obtained by C-V measurement.

f (kHz)	V_o (V)	V_D (eV)	N_D ($\times 10^{15}$ cm^{-3})	E_F (eV)	E_m (kV/cm)	W_D (μm)	$\Delta\Phi_B$ ($\times 10^{-4}$ eV)	Φ_B (eV)
1	0.23	0.25	1.98	0.24	11.75	0.39	3.93	0.49
2	0.45	0.48	1.83	0.24	15.93	0.57	4.57	0.72
3	0.49	0.52	1.84	0.24	16.69	0.59	4.68	0.76
5	0.48	0.50	1.77	0.24	16.10	0.59	4.60	0.74
7	0.49	0.51	1.75	0.24	16.16	0.60	4.60	0.75
10	0.48	0.50	1.79	0.24	16.23	0.59	4.61	0.74
20	0.48	0.51	1.74	0.24	16.02	0.60	4.58	0.74
30	0.50	0.53	1.75	0.24	16.42	0.61	4.64	0.77
50	0.49	0.52	1.67	0.24	15.85	0.62	4.56	0.76
70	0.48	0.50	1.67	0.24	15.63	0.61	4.53	0.74
100	0.57	0.59	1.63	0.24	16.77	0.67	4.69	0.83
200	0.55	0.57	1.67	0.24	16.72	0.65	4.68	0.81
300	0.60	0.62	1.65	0.24	17.40	0.69	4.78	0.86
500	0.65	0.67	1.65	0.24	18.07	0.71	4.87	0.91
700	0.66	0.69	1.58	0.24	17.93	0.74	4.85	0.93
1000	0.31	0.34	1.53	0.24	12.08	0.52	3.98	0.58

voltage ($V_0 = V_D$–kT/q) as follows,

$$N_D = 2/(q\varepsilon_0\varepsilon_s A^2 \tan\theta) \tag{18}$$

$$W_d = (2\varepsilon_s V_D/qN_D)^{1/2} \tag{19}$$

Table 2 introduces the electronic parameters of the MIS structure in the frequency range of 1kHz-1MHz obtained by the C-V measurement. The presence of an insulator layer at the interface of M/S, series resistance (R_s), and surface state density (Nss) results in a high intercept voltage. Moreover, the R_s quantity is more effective at higher frequencies while the N_{ss} factor plays a crucial role at lower frequencies [23, 37].

The frequency-dependent of the MIS structures conductivity is given by [35, 36]:

$$\sigma = \left(\frac{d_i}{A}\right)\omega C \tan\delta = \varepsilon_0\varepsilon''\omega \tag{20}$$

The profile of σ as a function of applied bias voltage for the MIS structure at the frequency range between 1 kHz to 1 MHz and room temperature is presented in figure 10(a). The value of the parameter σ increases with increasing frequency, in contrast to the parameters ε' and tan δ. This means that the electrical conductivity of the structure only affects the dielectric loss, which is infinite at zero frequency and negligible at high frequencies [32]. As the applied bias voltage rises, the electrical conductivity increases due to a decrease in polarization. This, in turn, leads to a rise in eddy current and a corresponding increase in energy loss tan δ [30].

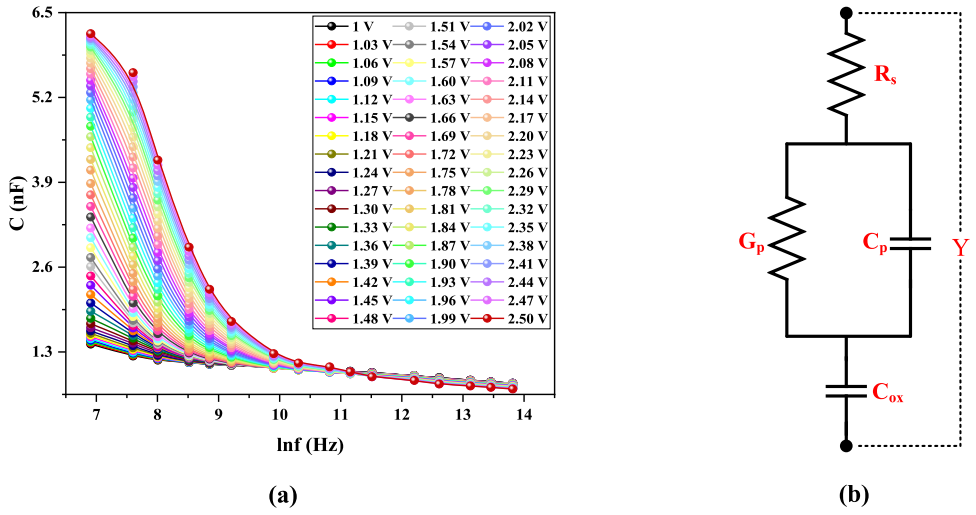

Figure 11. The changes of (a) C-ln(f) profiles and (b) equivalent circuit diagram for the MIS sample.

Using an AC voltage signal (V_{ac}) and a DC voltage applied, the C-V measurements for MIS sample are performed as depicted in figure 5(a). The N_{ss} is able to easily track the AC signal at lower frequencies, while it does not have this ability at higher frequencies. It must be noted that the period of AC signal is equal to $T = 1/2\pi f$ and the lifetime of charges is higher than τ in the trap. So, the high (C_{HF})-low (C_{LF}) frequency capacitance technique is employed in this work to calculate the N_{ss} profile as [15, 16];

$$N_{ss} = \frac{1}{qA}\left[\left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1}\right] \tag{21}$$

The voltage-dependent N_{ss} profile has been represented in figure 10(b). The N_{ss} profile of the MIS structure has a maximum value in the voltage range between −4.5 V and 0.15 V, equal to 3.18×10^{12} $eV^{-1}.cm^{-2}$. However, it is almost constant at the negative bias region from −4.5 V to −0.5 V, equal to 2.00×10^{9} $eV^{-1}.cm^{-2}$.

3.4. Frequency-dependent Impedance (C/(G/ω)-f) of the sample

The capacitive feature of the MIS structure was investigated by measuring its frequency-dependent impedance at applied bias voltages ranging from 1.00 V to 2.50 V and frequencies from 1 kHz to 1 MHz. The changes in capacitance and frequency value at room temperature for the MIS structure are shown in figure 11(a). At higher frequencies, the dispersion effect causes electrical charges in surface states and concert with the semiconductor to not affect the capacitance, meaning that the AC signal is not tracked [40]. As a result, the MIS structure's capacitance value exponentially changes with the frequency. Figure 11(b) shows the equivalent circuit diagram for the Al/SiO_2-surfactant/n-Si MIS structure.

Moreover, the profiles of G/ω-f can indicate the energy distribution of surface states (see figure 12(a)). At higher frequencies, the electric field cannot be adequately accounted for by the dipole moments, resulting in a decrease in G/ω as frequency increases [41]. According to the Nicollian and Brews, the parallel conductance (G_p/ω) is given by [23, 34];

$$G_p/\omega = \frac{\omega C_m C_i^2}{{G_m}^2 + \omega^2 (C_i - C_m)^2} = \frac{qN_{ss}}{2\omega\tau} \ln\left[1 + (\omega\tau)^2\right] \tag{22}$$

with τ being the relaxation time of the surface states, ω the angular frequency, C_i the capacitance of the interfacial layer, C_m and G_m the quantity of capacitance and conductance measured at each bias voltage, respectively. Figure 12(b) illustrates the G_p/ω-ln(f) profiles in the bias voltage range of 1.00 V-2.50 V with a step of 0.03 V at room temperature. A sharp peak is observed at each bias voltage whose position moves towards larger frequencies by increasing the applied bias voltage.

In addition, the peak value of G_p/ω-ln(f) profiles is able to be used to calculate the surface state density (N_{ss}) and their relaxation time at each bias voltage as follows;

$$N_{ss} = \frac{(G_p/\omega)_{max}}{0.402qA} \tag{23}$$

It must be noted that the $\omega\tau$ value is 1.98. Figure 13(a) represents the evolution of the N_{ss} profile in terms of applied voltage in the frequency range between 1 kHz and 30 kHz. Its maximum and minimum values are

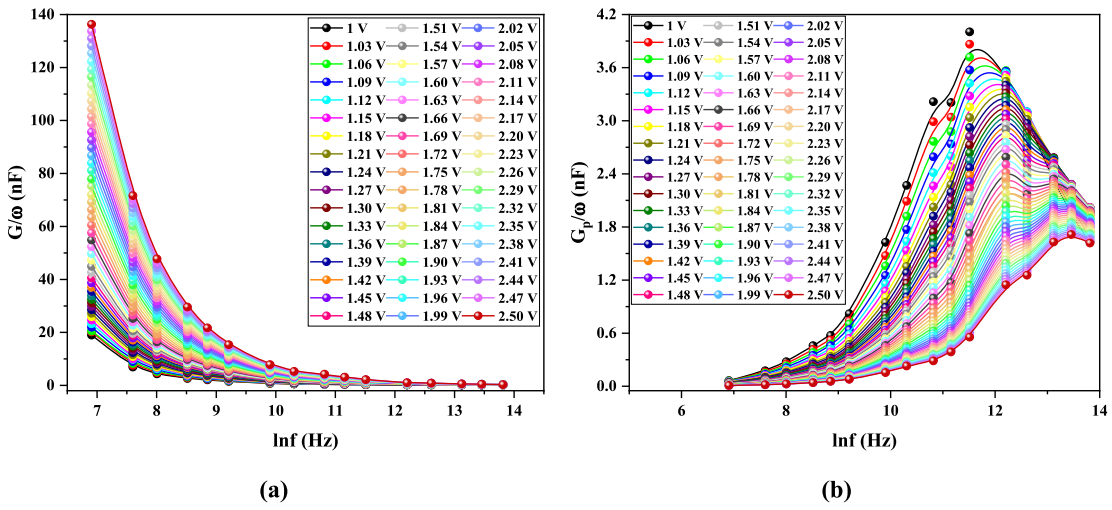

Figure 12. The changes of (a) G/ω and (b) G_p/ω versus frequency for the MIS sample.

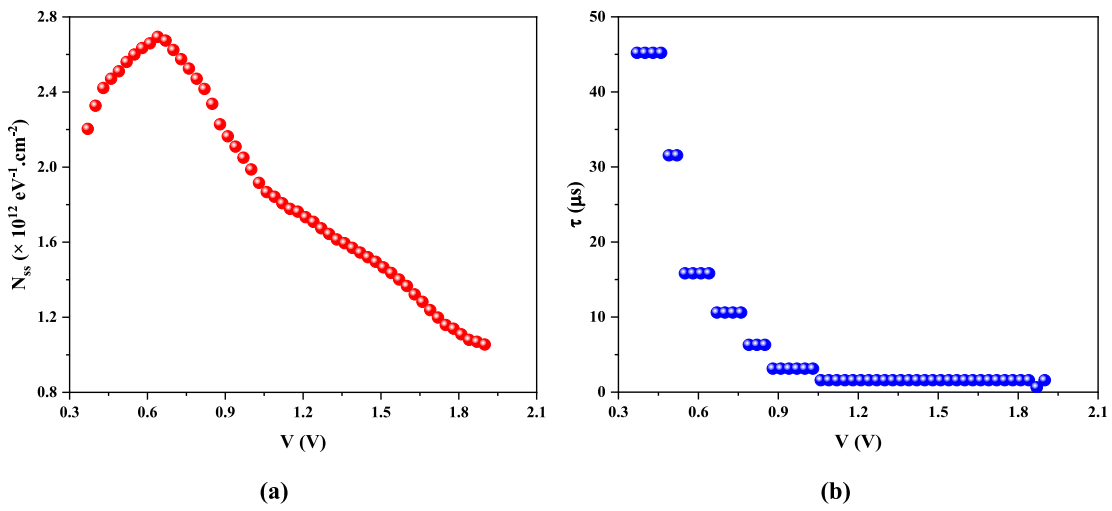

Figure 13. The changes of (a) N_{ss} and (b) τ versus applied voltage for the MIS sample.

2.69×10^{12} $eV^{-1}.cm^{-2}$ and 1.05×10^{12} $eV^{-1}.cm^{-2}$ occurred in the applied voltage of 0.64 V and 1.90 V, respectively. The relaxation time was also computed in this frequency range and its voltage-dependent profile is shown in figure 13(b). The value of τ decreases exponentially, from 45 μs at 0.37 V to 15 μs at 1.9 versus

Figure 14(a) illustrates the variation of ε' with frequency at applied bias voltages ranging from 0.25 V to 4 V, frequencies from 1 kHz to 1 MHz, and room temperature. It is evident that the plots reach a minimum value of 100 kHz and remain constant as the frequency rises. At lower frequencies, the stored energy in the MIS structure increases significantly when the applied bias voltage is increased, particularly at 4versus At higher frequencies, the stored energy remains relatively constant for all applied voltages. Moreover, the polarization is reduced at higher frequencies, resulting in ε' decreasing with frequency as N_{ss} cannot fall into step with the AC signal at higher frequencies and eventually reaches a constant value. The reason for this is that the electrons cannot follow the alternating field beyond a specific frequency of the external field [36]. Figure 14(b) demonstrates the frequency-depend imaginary part of the complex permittivity ε'' at applied bias voltages ranging from 0.25 V to 4 V, frequencies from 1 kHz to 1 MHz, and room temperature. At lower frequencies, the energy loss in the MIS structure reduces with the increase of the applied bias voltage. As seen, the maximum energy loss is related to the highest applied voltage of 4versus As the frequency increases and the energy loss decreases to a constant value, the effect of applied bias voltages is diminished. The reason why the main response of the MIS structure is observed at lower frequencies is that the grain boundaries have high resistance [42].

Figure 15(a) illustrates the changes in tan δ versus frequency at applied bias voltages ranging from 0.25 V to 4 V, frequencies from 1 kHz to 1 MHz, and room temperature. It is clear that the maximum value of tan δ for all

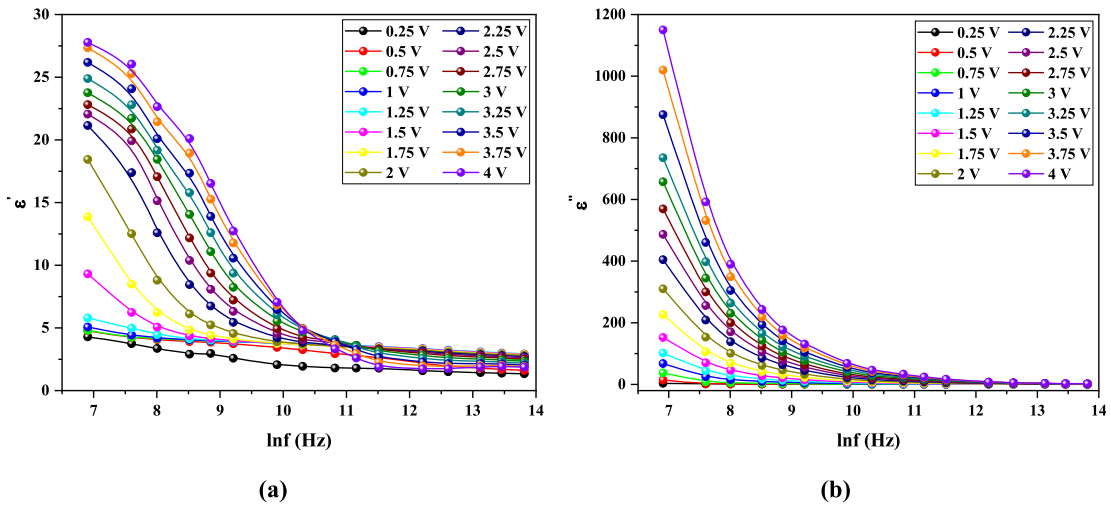

Figure 14. The function of (a) ε' and (b) ε'' versus frequency for the MIS sample.

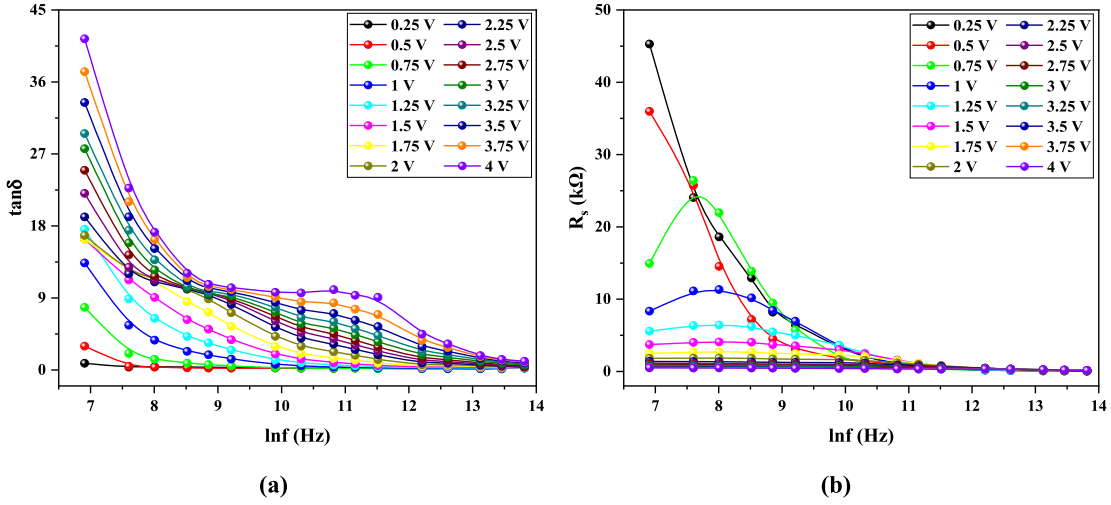

Figure 15. The curves (a) tan δ and (b) R_s versus frequency for the MIS sample.

the applied bias voltages appears at the frequency of 1 kHz and then intensely decreases. Moreover, the greatest and smallest values of the loss tangent at the frequency of 1 kHz are respectively related to 4 V and 0.25 V in the applied voltage range.

The variations of the frequency-dependent R_s at applied bias voltages ranging from 0.25 V to 4 V, frequencies from 1 kHz to 1 MHz, and room temperature are depicted in figure 15(b). As seen, the R_s profiles for the MIS structure at all applied bias voltages have an extreme value at the frequency of 1 kHz, but they significantly reduce at the higher frequencies. At the frequency of 1 kHz, the minimum and maximum values of R_s correspond to the applied bias voltages of 4 V and 0.75 V, respectively. It must be noted that the charges at interface traps can track the AC signal at low frequencies, resulting in a real contribution to the signal's value as well as series resistance [40, 41].

It is useful to mention that the power law is tracked by the electrical conductivity as follow [38, 39]:

$$\sigma = \sigma_0 + A\omega^{s_1} + B\omega^{s_2} \tag{24}$$

where σ_0 is the DC part, ω is the angular frequency (2πf), and s_1 and s_2 are dimensionless frequency exponents that provide insight into the conduction mechanisms of the MIS structure. The powers of s_1 and s_2 are the slope of the ln(σ)-ln(ω) graph. Figure 16(a) presents the frequency-dependent electrical conductivity of the MIS structure at applied bias voltages ranging from 0.25 V to 4 V, frequencies from 1 kHz to 1 MHz, and room temperature. The minimum interfacial polarization occurs at higher frequencies, leading to higher electrical conductivity. In addition, the increment of the eddy current and the energy loss causes the growing σ up. These processes are more effective at higher voltages applied [39]. In addition, the ln(σ) profile for the MIS structure at

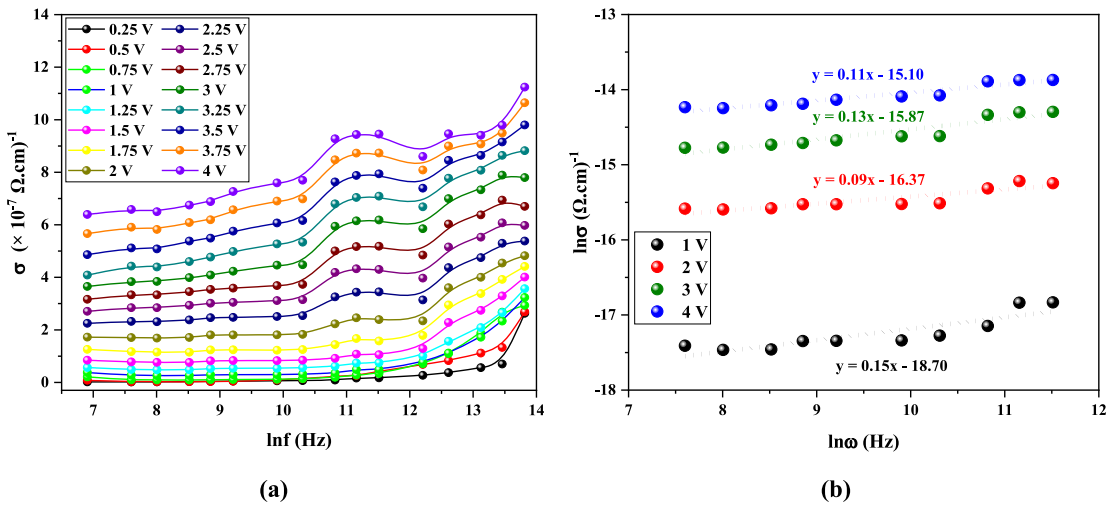

Figure 16. The profile of (a) σ versus frequency and (b) the ln(σ)-ln(ω) for the MIS structure.

the applied bias voltages of 1 V, 2 V, 3 V, and 4 V is demonstrated in figure 16(b). As can be observed, these profiles are linear whose slopes are reduced by increasing the selected applied bias voltages. Similar results on the interfacial layer, impedance frequency, and dielectric properties have been already also reported in the literature [38, 39, 43–46]

Similar results have also been reported in the literature by various researchers regarding the MS structure, both with and without a SiO_2 interfacial layer, utilizing different growth techniques [10, 11, 45, 47–49]. However, these studies generally focus on a narrow or single voltage and frequency range and do not compare them with the standard MS diode. Typically, surface state values are extracted from the forward bias I-V data, and a thin SiO_2 layer is formed either as native or through the classic thermal oxidation method.

To obtain more detailed, accurate, and reliable results on these devices, it is necessary to conduct electrical measurements across a wide range of voltages, temperatures, and frequencies using various measurement techniques. Discrepancies in the basic electrical parameters obtained from forward bias I-V and reverse bias C-V data using different calculation methods can arise due to their voltage dependence and the nature of the BH M/S interface.

Among these studies, H. Kanbur *et al* examined the effects of N_{ss} and excess capacitance on the electrical characteristics of an MIS structure with a 3.2 nm native SiO_2 interlayer. We also conducted a systematic investigation into the frequency dependence of the electrical properties of these structures within a narrow frequency range (0.1–1 MHz). Additionally, the N_{ss} versus (E_{ss}-E_v) profile was derived solely from the forward bias I-V data, considering the voltage-dependent barrier height and ideality factor [47].

M Okutan and F Yakuphanoğlu attempted to investigate the detailed electrical transport properties of an Ag/SiO_2/n-Si (MIS) diode with a 3.61 nm native SiO_2 interlayer using forward bias I–V characteristics and impedance spectroscopy measurements. Their study provided evidence of non-ideal behavior in the Ag/SiO_2/n-Si diode due to the oxide layer, as well as R_s and N_{ss} modifying the electrical characteristics of the diode. Basic electrical parameters such as diffusion potential, donor atom doping, Fermi energy, and BH were calculated for only 1 MHz, with the N_{ss} versus (E_c-E_{ss}) profile extracted solely from the forward bias I-V data, considering the voltage-dependent BH and n [48].

In a separate study, M L Grili *et al* fabricated Ni/TiO_2/p-Si/Al structures with 103 nm and 84 nm thick TiO_2 interlayers [49]. They noted that the rectifying properties of these structures improve as the TiO_2 film thickness increases, similar to our findings. The Al/SiO_2/n-Si (MIS) structure in our study exhibited a good rectification ratio (RR = I_F/I_R) with C-V curves resembling those of a MOS structure. While the MIS structure inherently features a capacitor, if an interface layer with a thickness of 500 nm is present, it no longer exhibits I-V characteristics, and thus is referred to as a MOS capacitor rather than a MOS diode.

In the present study, we fabricated both the Al/n-Si (MS) and Al/SiO_2/n-Si (MIS) structures on the same n-Si wafer to investigate the effect of the SiO_2 interlayer grown by the spin coating technique on basic electrical parameters and conduction mechanisms. We employed I-V and C/G-V-f measurements across a wide voltage and frequency range to obtain more accurate and reliable results on both electric and dielectric properties.

Specifically, we obtained voltage-dependent profiles of N_{ss} and R_s, which negatively impact both electrical and dielectric properties, using the parallel conductance method developed by Nicollian-Brews and Nicollian-

Goetzberger, respectively. The conductance method is highly sensitive and provides more accurate and reliable results on N_{ss} and their lifetimes or relaxation times due to the requirement for multiple C-V-f and G-V-f plots.

In contrast, the forward bias I-V method only requires a single I-V plot, and the low-high frequency C-V method necessitates just two C-V plots, thereby offering limited information on N_{ss} compared to the conductance method. The possible CCMs, such as ohmic, SCLC, and TCLC, were identified from the double logarithmic forward bias I-V plots, while Schottky/Frenkel Poole emissions were determined from the reverse bias I_R-$V_R^{0.5}$ plots for each diode. Furthermore, in this study, we analyzed the real and imaginary components of the complex dielectric (ε^*) and complex electric modulus (M^*), loss tangent (tanδ), and AC conductivity (σ) values as a function of frequency and voltage.

4. Conclusions

In this work, a MIS type SD with a structure of Al/SiO_2-surfactant/n-Si was made on the n-Si wafer. The detail of the deposition of the SiO_2-surfactant layer at the interface of M/S was explained. The fundamental electronic parameters of the MIS structure as I_0, BH, n, $R_{sh,}$ and R_s were computed by measuring the I-V data at room temperature and using different computation techniques, like, TE, Norde, and Cheung. The amounts of I_0, BH, n, R_s, R_{sh}, and RR for the fabricated MIS structure were obtained to be 1.13×10^{-8} A, 0.80 eV, 3.14, 2.06 kΩ, 20.93 MΩ, and 10.15×10^3, respectively. It was found that the SiO_2 insulator layer among the metal and semiconductor causes a reduction in the leakage current, ideality factor, interface states, and an increment of potential BH, shunt resistance, and RR. The observed discrepancies between fundamental electrical parameters as n, and R_s computed by the TE, Cheung, and Norde functions are the result of voltage-dependent values or calculation methods that correspond to different voltage and current ranges. Moreover, the incorporation of the SiO_2 insulator layer decreases the N_{ss} for the MIS-type SD compared with MS-type SD, resulting in the passivation of the semiconductor surface. When the theoretical and experimental values of the βPF amount were compared, it was found that the PFE mechanism was dominant in the MIS structure, while the SE process was dominant in the MS structure.

Additionally, the dielectric properties of the MIS structure depend on voltage and frequency that have been examined by the impedance measurement in the voltage range of 0.25V-4V and frequency range of 1kHz-1MHz at room temperature. The MIS structure dielectric features were increased by growing the bias voltage up contrary to the frequency raising. The inversion, depletion, and accumulation regions appeared in the voltage-dependent dielectric properties of the MIS structure. Such behaviors are due to the R_s and N_{ss} at the interface of the MIS structure. Besides, it was seen that the quantities of C and G/ω were significantly changed at the smaller frequencies while they did not depend on the frequency at the larger frequencies. Similar behavior was also observed in the other dielectric parameters, i.e., ε', ε'', tan δ, and R_s functions. The inability of electrons to follow the electric field is the main reason behind this behavior. It was observed that the σ value of the MIS structure is increased by the growing frequency up due to the reduction of interfacial polarization and the increment of the eddy current and energy loss.

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Data availability statement

The data cannot be made publicly available upon publication because they contain sensitive personal information. The data that support the findings of this study are available upon reasonable request from the authors.

Author contributions

Halil İbrahim Efkere: Investigation, Experimental, Visualization, Formal Analysis, Writing—review And editing. **Ali Barkhordari**: Visualization, writing. **Benedetta Marmiroli:** Investigation, Experimental, Review. **Barbara Sartori:** Investigation, Experimental, Review. **Süleyman Özçelik:** Review and editing, and Supervision. **G. Pirgholi-Givi:** Visualization, Writing. **Şemsettin Altındal**: Review and editing. **Yashar Azizian-Kalandaragh:** Investigation, Formal Analysis, Writing-review and editing.

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