The current–voltage (I–V) characteristics and low–high impedance measurements (C/G–V) of Au/(AgCdS:PVP)/n-Si Schottky diode (SD) at dark and under illumination conditions

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ABSTRACT

In this study, Schottky diode (SD) with a structure of Au/(AgCdS:PVP)/n-Si has been fabricated and then its electrical parameters and conduction mechanisms (CMs) investigated by measuring current–voltage (I–V) and capacitance/conductance–voltage (C/G–V) data in dark and under 100-mW cm^{-2} illumination intensity at room temperature (RT). These measurements show that almost all basic electrical parameters and CM depend on illumination, frequency, and voltage. The energy/voltage-dependent profile of surface states (N_{ss}) was extracted from the forward bias I–V data considering voltage dependence of ideality factor (n), barrier height, and low/high-frequency capacitance model. The density of doping atoms (N_d), barrier height (Φ_B(C–V)), and the width of depletion region (W_d) were also computed by the linear zone of the reverse bias C^{-2}–V plot at a frequency of 1 MHz, and the dark conditions. The maximum photosensitivity and photoresponsivity were found as 384 and 7.5 mW A^{-1} under 100 mW cm^{-2}, respectively. Based on the experimental findings, the Au/(AgCdS:PVP)/n-Si SD has good rectifier and photodiode behavior and hence, it can be successfully used in electronic and optoelectronic applications rather than conventional metal–semiconductor (MS)-type SD with/without an insulator layer grown by traditional techniques considering the advantages of polymers, such as high mechanical strength, low-cost production, and low energy consumption.

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1 Introduction

Diodes/photodiodes, solar cells (SCs), and capacitors formed by metal–(insulator/polymer/ferroelectric)–semiconductor (MIS, MPS, MFS) structures are the cornerstones of the semiconductor and electronics industries [1–10]. Although many theoretical and experimental studies have been performed on these devices for more than five decades, there is not a clear consensus among scientists regarding their conduction mechanisms (CMs), electrical/optical properties, the nature of potential BH, and surface/interface states density (N_{ss}). In addition, the scientific/technical problems of these structures are related to the improvement of device performance or quality, reduction of their cost, and the use of easy production mechanisms. Several variables affect the device efficacy of MIS-, MPS-, and MFS-type Schottky structures; like the surface preparation of the semiconductor wafer, the growth of the interlayer (its thickness, homogeneity, and dielectric constant), the nature of the BH, applied voltage, series & shunt resistances (R_s, R_{sh}), N_{ss}, n, frequency, illumination, and temperature [11–14]. Among these, N_{ss} is indeed an unwanted device feature since it acts as a recombination center and causes serious influences on the I–V and C/G–V characteristics.

Conventional thermionic emission (TE) theory fails to extract these device parameters from the I–V and C/G–V data as they are also affected by operation conditions like temperature, frequency, and radiation. The I–V and C/G–V profiles generally show various behaviors at low, intermediate, and higher voltages because of the effects of R_s, N_{ss}, and interlayer. Among these, the effect of N_{ss} on the I–V and C/G–V characteristics is prominent at intermediate bias voltages, but the characteristics at higher bias voltages are affected by R_s and the interlayer in a stronger way. Therefore, the I–V and C/G–V profiles at forward bias show a concave curvature at high bias voltages since the total bias voltage on the circuit is contributed by the depletion layer, interlayer, N_{ss}, and R_s of the device [3–5, 11–17]. The value of n is usually much higher than the unity ($n > 1$), indicating the device does not conform with the conventional TE theory. As a result, both BH and n depend on the voltage when it is forward biased. Since the thickness of the interlayer becomes higher than a few nanometers, N_{ss} is in equilibrium with semiconductors, and they are quite effective in the CMs in these devices [18–23].

Under the illumination ($hc/q\lambda \geq E_g$), more electron–hole pairs are created at the junction or near the depletion region of the SDs. After that, these electronic charges will be moved in opposite directions of the interior electric field ($\mathbf{F} = \pm q\mathbf{E}$) and thus create a net photocurrent on the circuit. These separations of electron–hole pairs become more dominant when the device is reverse-biased. Because the external and internal electric fields are in the same direction in the inversion region, a higher total electric field is observed compared with the forward bias region. As a result, the value of photocurrent in the reverse biases is considerably higher than that of in forward biases. Thus, an increased number of charge carriers causes some enhancements in photoconductivity and responsivity, which are considered the measure of the performance in terms of sensitivity to light. It must be noted that polymers have low permittivity and conductivity, but they can be enhanced/adjusted by adding some metal/metal-oxides into the polymer in appropriate proportions. The more commonly used polymers in these devices as interlayer materials are usually polyvinyl-alcohol/pyrrolidone (PVA/PVP), polyvinyl-acetate (PVAc), and poly-aniline/pyrrole (PANI, PPy). Among them, similar functional groupings exist in PVP/PVA and hence, they are compatible with cross-linking. The PVA is semi-crystalline and the PVP is amorphous while both are water-soluble [19–26].

In general, conventional MS-type devices with an insulator interlayer grown by traditional techniques cannot completely passivate the active dangling bonds at the semiconductor surface. The fabrication is also quite dependent on surface preparation, deposition of the interlayer, its thickness/homogeneity, and dielectric value. But the usage of a thin interlayer with high-dielectric at the M–S interface, can quite reduce the inter-diffusion between them, isolate them from each other, passivated many N_{ss}, leakage current, and can gain a capacitor behavior of them so more storage electrons/energy, and high breakdown voltage. Today, the basic scientific/technical problems of these devices are to increase efficiency/performance and to reduce energy losses, and cost production of them. The analysis of the I–V characteristics only at room/narrow voltage and temperature range cannot supply us with more accurate/reliable information on the possible conduction mechanisms, and the formation of nature/homogeneity BH at the M–S interface. However, simultaneous contribution from two or

more conduction mechanisms like TE, TFE, FE, tunneling mechanism via surface states, anomaly, and Gaussian distribution of BH could also be possible in certain voltage and temperature ranges [1, 11–16]. However, FE and TFE may be dominated only at low-temperature and high doping concentrations of donor/acceptor atoms [3–5, 15]. Since these measurements were performed in large bias voltage and illumination could allow us to gain insight into different aspects of characteristics such as CMs, nature of BH, and deposited interfacial layer.

In this study, the first aim is to prepare a MPS type SD that has the structural form of Au/(AgCdS:PVP)/n-Si and investigate its basic electrical parameters using the I–V and C/G–V measurements at room temperature in a wide voltage range in dark and 100 mW cm^{-2} illumination intensity. The second aim is to explore the effects of R_s, N_{ss}, and the organic interlayer on the I–V and C/G–V data. The observed discrepancies regarding the electrical parameters of the device were associated with the nature of BH between Au and n-Si, a spatial density distribution of N_{ss} between (AgCdS:PVP) interlayer and n-Si, and the nature of the calculation method of TE, Cheung, and Norde model.

2 Experimental procedures

In this research, Au/(AgCdS:PVP)/n-Si MPS-type SD was grown onto an n-Si (phosphorus-doped) wafer which has about 350 μm thickness, 5.08 cm diameter, and 1–10 Ω cm^{-1} resistivity. To remove any native-oxide layer and other dirties from the n-Si wafer, it was rinsed in ammonium peroxide for 1 min. Consequently, it was rinsed in a chemical solution of (H_2SO_4:H_2O_2:H_2O) with a ratio of 3:1:1 and (HCl: H_2O) with a ratio of 1:1 for one minute in the ultrasonic bath to etch the wafer. After that, the wafer was rinsed in the high-resistivity deionized water and dried with high-purity N_2 gas. Later, the wafer was taken into the chamber of the thermal evaporation system and the air was vacuumed until the chamber reached 10^{-6} Torr. Then, pure Au (99.999%) was evaporated onto the backside of the wafer with 150 nm thickness was grown onto the backside of the n-Si wafer. To obtain a low resistivity an ohmic back contact, n-Si/Au wafer was annealed at 500 °C for 5 min in the nitrogen atmosphere.

For preparing polymeric interlayer, the PVP with an average molecular weight of 130.000 g mol^{-1} is purchased from Sigma-Aldrich. The PVP powder was dissolved in deionized water with a weight-per-weight ratio of 8% at 80 °C, keeping the solution stirred for about 3 h, and then the prepared solution was left at room temperature for cooling. Next, Ag and CdS nanostructures were mixed into the solution and the front surface of the n-Si wafer was coated with the polymeric solution using sputtering technique. The interlayer thickness was estimated at 60 nm using the interlayer capacitance. Finally, highly pure Au (99.999%) was grown onto (AgCdS:PVP) interlayer using a shadow mask so that rectifier contacts with a 150 nm thickness were formed under the same high-vacuum thermal evaporation system. Finally, the impedance measurement was performed utilizing an HP4192A LF impedance analyzer between 3 kHz and 1 MHz. The I–V data were measured by a Keithley-2400 sourcemeter in the dark and under 100 mW cm^{-2} illumination intensity.

3 Result & discussions

3.1 The I–V characteristics of fabricated SD

Figure 1 represents the semi-logarithmic I–V plots of the SD at dark and under illumination conditions. It is clear that the Ln(I) vs V plots have large sections that exhibit linearity in the moderate voltages for both conditions. As shown in these plots, the reverse current for dark conditions does not show any soft saturation behavior, whereas that for illumination conditions has a good saturation behavior. Such non-saturation of current for the dark condition can be because of the generation-recombination process of the electron–hole pairs and the image-force lowering of the barrier height (BH). The electrical and optical properties of the SD are exceptionally related to the light intensity, electric field, and interlayer, so the analysis of the SD should be performed not only in the dark but also under illumination to supply more reliable and accurate information. When the linear region of the forward bias Ln(I)–V plot becomes much smaller, the reliability and accuracy of the extraction of the electrical parameters may be questionable. For this case, Cheungs' and Norde's functions may be used as an alternating method to obtain basic electrical parameters (n, R_s, and Φ_B) in the dark and under illumination conditions [7–10, 15].
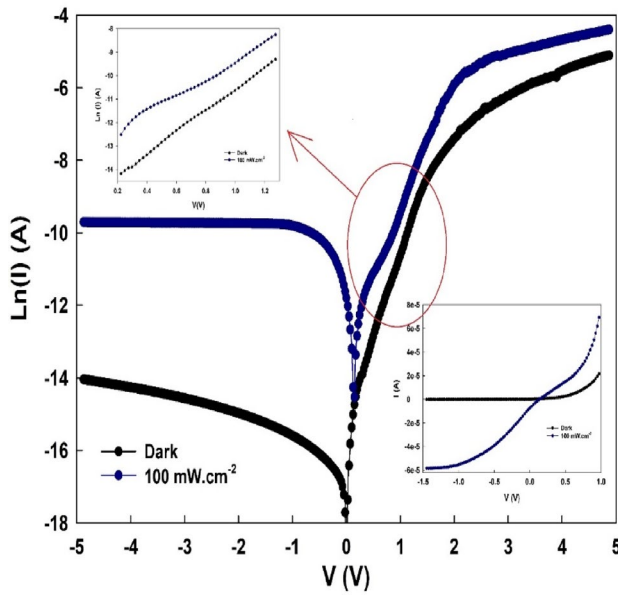
Fig. 1 The I–V curves of the fabricated SD in the dark and under an illumination intensity of 100 mW cm^{-2}

Ascan be seen in Fig. 1, the linearity is observed only at a small bias voltage range of Ln(I) vs V curves whereas for the rest of the voltages, deviations occur because of R_s and polymeric interlayer, resulting in dividing the total voltage applied on the SD between the polymeric interlayer, R_s, and depletion layer of the SD ($V_a = V_i + V_{Rs} + V_d$). The illumination causes the generation of electron–hole pairs to create a photocurrent in the whole bias region, thus the current passing through the device is increased. However, the fabricated SD is very sensitive to illumination under reverse bias voltages due to the same direction of the interior and external electric fields in contrast to the positive voltages and hence, the total electric field for the reverse-biased device is higher. As a result of the higher electric field in this region, the recombination of electrons with holes is less noticeable. Thus, photocurrent is increased by pushing them in opposite directions.

When an MS-type SD with and without an interlayer has an R_s and an ideality factor higher than 1, the basic electrical parameters of this type of device, such as saturation current (I$_s$ or I$_0$), n, zero, or voltage-dependent BH ($\Phi_B(I–V)$) can be calculated using the forward bias I–V data in the following expression based on the TE model ($V_F \geq 3kT/q$) [3–5]:

$$I(V) = I_0 \left[\exp \left(\frac{q(V - IR_s)}{nkT} \right) - 1 \right] \quad (1a)$$

At room and above temperatures, the value of − 1 in Eq. 1(a) can be neglected with respect to the exponential term and the IR$_s$ can be also ignored when compared with applied bias voltage. In this case, for the linear part of the Ln(I)–V plot, Eq. 1(a) can be rearranged as Ln(I) = Ln(I$_0$) + (q/nkT). In this equation, the quantities of I$_0$, IR$_s$, T, and k are the reverse saturation current at zero bias voltage, the voltage drop on the R$_s$, the temperature in K, and the Boltzmann constant, respectively. Since the Ln(I)–V plot exhibits a nearly linear behavior for the intermediate bias voltages, it is possible to calculate I$_0$ using the intersection point of this plot as given by [2, 3, 15].

$$I_0/(SA^*T^2) = \exp \left(\frac{-q\Phi_B}{kT} \right) \quad (1b)$$

Here, S and A* quantities are the area of Schottky contact and the Richardson constant which is considered to be 112 A (cm^{2}K^2)$^{-1}$ for n-Si, respectively. Using the extracted value of I_0, Φ_B is obtained as follows [3–5]:

$$\Phi_B = \left(\frac{kT}{q} \right) \ln \left(\frac{SA^*T^2}{I_0} \right) \quad (1c)$$

Another important SD parameter is the n which is also extracted by the slope of the linear part of Ln(I)–V curve as [3–5]:

$$n = \frac{q}{kT\tan(\theta)} = \left(\frac{q}{kT} \right) \frac{dV}{d\text{Ln}(I)} \quad (1d)$$

Thus, the calculated basic electrical parameters of prepared Au/(AgCdS:PVP)/n-Si MPS-type SD are listed in Table 1. As can be observed, the basic electrical parameters are strong functions of illumination intensity as well as bias voltage. The value of n is more than one both in the dark and under 100 mW cm^{-2}. Such high values of n are explained by the presence of (AgCdS:PVP) polymeric interlayer, N$_{ss}$, W$_d$, barrier inhomogeneity, and image force lowering of BH which are related to each other as follows [7–11, 15]:

$$n(V) = 1 + \frac{d_i}{\varepsilon_i} \left[\frac{\varepsilon_s}{W_d} + qN_{ss} \right] \quad (2)$$

The barrier inhomogeneity at the M/S interface like the lower patches around the mean BH may

Table 1 Electrical features of the fabricated SD in low/moderate bias region (LBR/MBR) at dark and under an illumination of 100 mW cm^{-2}

Power (mW cm^{-2})	Region	TE					Ohm's law		Norde function		Cheung functions			
											dV/dln(I)		H(I)	
		n	I_0 (A)	Φ_{B0} (eV)	RR $\times 10^3$		R_s (kΩ)	R_{sh} (MΩ)	Φ_{B0} (eV)	R_s (kΩ)	n	R_s (kΩ)	Φ_{B0} (eV)	R_s (kΩ)
Dark	LBR	7.85	2.21×10^{-7}	0.69	7.73		0.79	6.09	0.72	1.19	6.44	0.34	0.70	0.27
	MBR	8.56	2.72×10^{-7}	0.68										
100	LBR	5.28	7.09×10^{-7}	0.66	0.21		0.39	0.082	0.79	0.48	9.90	0.07	0.62	0.07
	MBR	13.81	3.66×10^{-6}	0.62										

be more effective on charge transport over the BH because they can be easily transported through the lower sections or patches of barrier and hence, the value of I_0 and n is increased with the increase of forward bias voltage.

Since the SD has sufficiently high R_s, the Ln(I)–V curve at high forward bias voltage has a nonlinear trend (Fig. 1). Greater values of R_s usually originated from the upper and back electrodes (Schottky/ohmic contacts), the probe wires used for electrical measurements, the semiconductor's bulk resistivity, and non-homogeneities of doping atoms into semiconductor [3, 15, 27]. There are a lot of methods for extraction of R_s from the I–V data at forward bias in the literature. Among them, the most used ones are the Norde function [28], the Cheung function [29], and Ohm's law [3]. In addition, the basic electrical parameters (n, R_s, Φ_B) can be extracted utilizing the Cheung functions as a second way [29]. It is noteworthy that the R_{sh} of these devices generally stems from the probe wires to the ground, some physical disorder/impurities, the leakage current paths along the interlayer at the device contacts, and the conductivity paths such as grain boundaries and dislocations. It is well known that the resistance (R_i) of these devices is strongly affected by bias voltage and its value was simply calculated utilizing Ohm's law ($R_i = dV_i/dI_i$), as illustrated in Fig. 2. It is clear that R_i becomes nearly voltage independent or almost constant for sufficiently high forward/reverse voltages at about ± 5 V. Therefore, we can say that the R_i values at + 5 V and − 5 V correspond to the real values of R_s and R_{sh}, respectively. As expected, R_s and R_{sh} decrease after illumination due to the increase of the conductivity. Because more and more electrons (N_q) can receive enough energy to stimulate from the
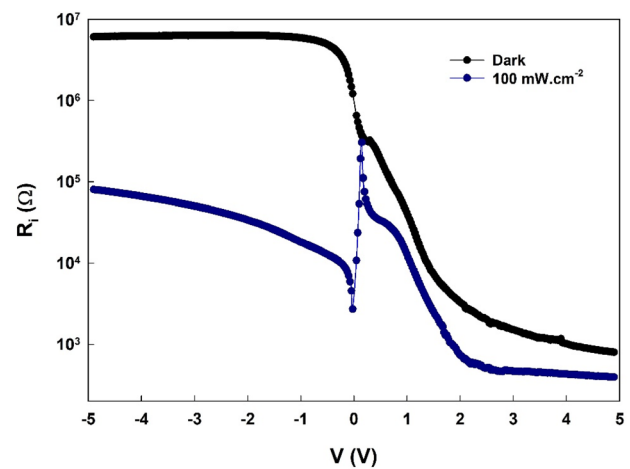
Fig. 2 The R_i–V plots of the prepared SD in the dark and under an illumination intensity of 100 mW cm^{-2}

valance band to the conduction band under illumination, the conductivity is enhanced.

Furthermore, n, R_s, and Φ_B can be obtained using the I–V data of the manufactured SD at sufficiently high voltages in the forward bias by the Cheung functions as follows:

$$\frac{dV}{dln(I)} = \frac{nkT}{q} + IR_s \tag{3a}$$

$$H(I) = V - \frac{nkT}{q}\ln\left(\frac{I}{SA^*T^2}\right) + IR_s \tag{3b}$$

Figure 3 shows the plots of dV/dln(I) and H(I) versus I. The calculated values of dV/dln(I) and H(I) exhibit linear dependence on current for sufficient current range. As shown in Fig. 3a and b, both the dV/dln(I) and H(I) versus I plots have good linear regions.
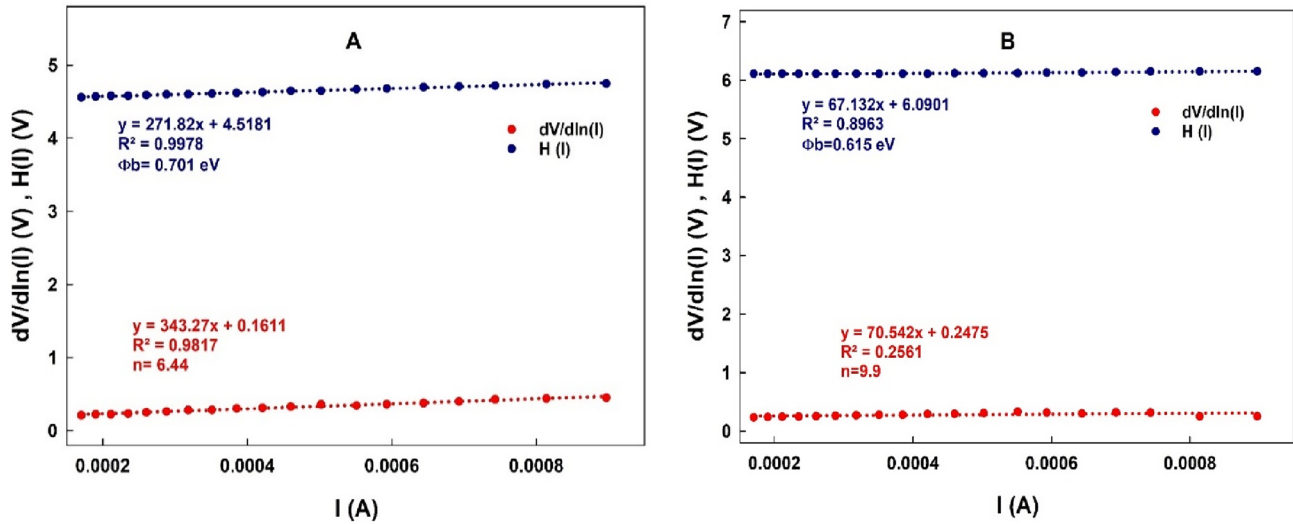
Fig. 3 The dV/dln(I) vs I and $H(I)$ vs I curves of the developed SD **a** in the dark and **b** under an illumination intensity of 100 mW cm^{-2}

Firstly, the slope and intercept point of the dV/dln(I)-I curves were used in Eq. 3(a) to find R_s and n, respectively. Secondly, $H(I)$ was calculated using the value of n in Eq. 3(b) so that the slope and intercept point of the $H(I)$-I curve were used to find R_s and Φ_B, respectively. The obtained results are also tabulated in Table 1. There are differences between the values obtained by TE theory and Cheung functions. It is believed to be due to the voltage dependence of these parameters and the nature of these different techniques which use different bias regions for parameter extraction.

Norde function can also be utilized to get electrical parameters, i.e., Φ_B and R_s [30]. The Φ_B and R_s values were obtained using Eq. 4(a). Therefore, the F(V) function was calculated using Eq. 4(a) for plotting it against bias voltage as depicted in Fig. 4. According to the Norde method, the F(V)–V plot exhibits a local minimum (see Fig. 4), and the values of BH and R_s can be calculated using the corresponding V_m and I_m values in Eqs. 4(a-c) which are given by

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left[\frac{I}{T^2 A^* A}\right]$$ (4a)

$$\Phi_B = F(V_{\min}) + \frac{V_{\min}}{\gamma} - \frac{kT}{q}$$ (4b)

$$R_s = \frac{kT(\gamma - n)}{qI_{\min}}$$ (4c)
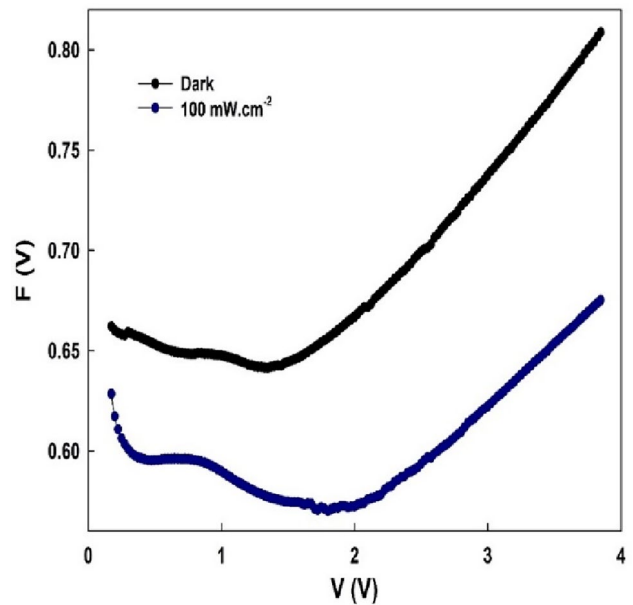

Fig. 4 The F(V)–V profiles of the fabricated SD at dark and under a light intensity of 100 mW cm^{-2}

where γ is a dimensionless integer, which must be chosen higher than n. Table 1 introduces Φ_B and R_s values calculated using Eqs. 4(b, c), respectively. There are some discrepancies in Table 1 regarding the values found using different methods. Such results can be associated with the used calculation methods (TE, Cheung, and Norde models), the voltage dependence of the parameters, a special distribution of N_{ss}, and barrier inhomogeneities at the M/S interface [3–11, 15].

It is clear that the obtained values of electric/optic parameters experimentally may be slightly different due to the nature of the measurement method and the voltage dependence of these parameters. For instance, the obtained value of BH from the reverse bias C^{-2} vs V plot is usually higher than the forward bias I–V data as almost Fermi energy. Because the apparent BH from the semiconductor to metal (F_B(I–V)) is lower than the metal to semiconductor ($= qV_{bi} + E_F$) for electronic charges, where qV_{bi} is the built voltage.

In general, N_{ss} originates from the preparation or cleaning processes of semiconductor wafers, surface imperfections, doping atoms, structural rearrangements because of metallization, and the interlayer at the M–S interface [26–28, 31]. The N_{ss} serves as a center for recombining charge carriers. Moreover, charge carriers can be caught or released under the effects of electric field and illumination. N_{ss} is quite effective on the I–V and C/G–V curves, particularly at moderate forward voltages. Several methods are available to obtain N_{ss}, such as Card–Rhoderick, high-low-frequency capacitance, and admittance methods [3–7]. In this study, both fast and reliable Card–Rhoderick and high-low-frequency capacitance methods were used. Card and Rhoderick [4] assert that n and BH are the voltage-dependent parameters. In addition, the ideality factor may get larger values than unity because of polymeric interlayer, N_{ss}, doping atoms, depletion layer width, and barrier inhomogeneity in accordance with the following equation [2–8];

$$n(V) = \frac{q}{kT}\left[\frac{(V - IR_s)}{\ln(I_i/I_0)}\right] = 1 + \frac{d_i}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right] \quad (5a)$$

Here, d_i is the interfacial layer thickness and ε_i and ε_s are the dielectric of interlayer and semiconductor, respectively. Additionally, W_D is the thickness of the depletion region which is calculated by the reverse bias C^{-2}–V at 1 MHz. Besides, the voltage-dependent BH parameter can be expressed as follows [4]:

$$\Phi_e - \Phi_{BO} = \alpha(V - IR_s) = \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \quad (5b)$$

with Φ_e being the effective-BH with voltage coefficient of $\alpha = d\Phi_e/dV = (1 - 1/n(V))$. Thus, the value of N_{ss} can be written as follows [4]:

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{d}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right] \quad (5c)$$

The energy states of N_{ss} at the surface of n-type semiconductors with respect to the conduction band's bottom (E_c) can be described by [3, 4, 15]

$$E_c - E_{ss} = q(\Phi_e - V) \quad (5d)$$

Thus, the energy-dependent profile of N_{ss} for the Au/(AgCdS:PVP)/n-Si MPS-type SD was obtained according to Eqs. 5(a–d) and shown in Fig. 5.

As can be observed from Fig. 5, the energy-dependent N_{ss} curves exhibit almost U-shaped behavior due to a spatial distribution of N_{ss} and their lifetimes (τ). These curves can be interpreted in such a way that N_{ss} increases exponentially from the middle of the bandgap (E_g) of the semiconductor to the bottom of the conduction band (E_c). Such behavior of N_{ss} in the E_g was attributed to an increase in donor states. On the other hand, the increase in the N_{ss} after the forbidden bandgap was attributed to the contribution of the acceptor traps.

To determine the possible CM at the forward bias region, such as ohmic, space charge limited current (SCLC), and trap charge limited current (TCLC), the double-logarithmic I–V plot of the prepared sample in dark and under an illumination intensity of 100 mW cm^{-2} was, respectively, given in Fig. 6A and B.

As shown in Fig. 6A and B, the $Ln(I_f)$-$Ln(V_f)$ plots have two distinct linear regions corresponding to the various current conduction mechanisms. The slope in regions I and II was found to be 2.077, 4.660 in the dark, and 1.676, 5.070 under 100 mW cm^{-2}, respectively. In region I, the CM at dark and under illumination is governed by SCLC, because
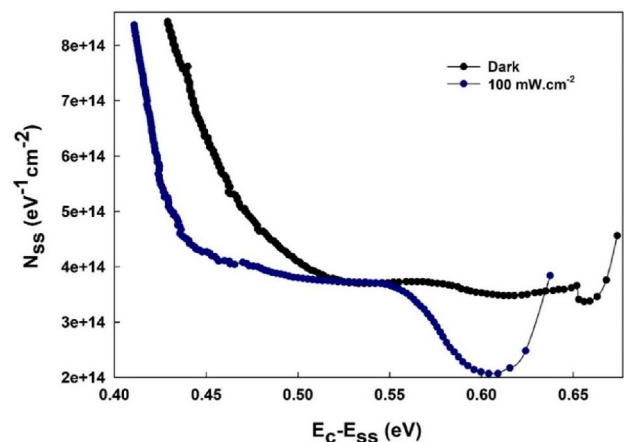

Fig. 5 The N_{ss} vs ($E_c - E_{ss}$) curves of the manufactured SD at dark and under a light intensity of 100 mW cm^{-2}
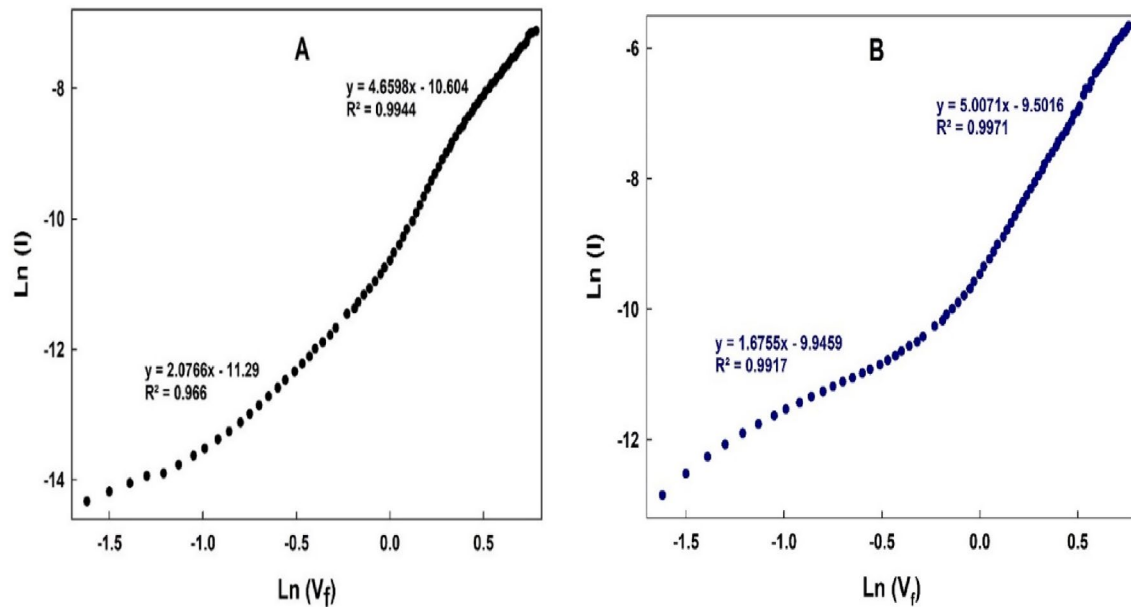
Fig. 6 The $\text{Ln}(I_f)$-$\text{Ln}(V_f)$ curve of the manufactured SD **a** in the dark and **b** under 100-mW cm^{-2} illumination

the slope is closer to 2. This is because more electrons are injected from the electrode to the semiconductor, filling up interface levels and increasing space charges [15]. In region II, indicating the dominance of the TCLC mechanism with an exponential trap distribution.

Both the photoresponsivity (R) and photosensitivity (S_{ph}) of the prepared SD with a structure of Au/(AgCdS:PVP)/n-Si under an illumination power of 100 mW cm^{-2} are obtained as follows:

$$R = \frac{I_{ph}}{P \times A} \tag{6a}$$

$$S_{ph} = \frac{I_{ph}}{I_{dark}} \tag{6b}$$

where the quantities of I_{ph}, I_{dark}, P, and A denote the photocurrent, dark current, illumination power, and rectifier contact area, respectively. The change in the voltage-dependent R and S_{ph} profiles was respectively depicted in Fig. 7a and b. The maximum values of R and S_{ph} under an illumination intensity of 100 mW cm^{-2} were found to be 7.5 mW A^{-1} and 384, respectively. This increment in photosensitivity stems from the photogenerated electrons and holes under illumination and the electric field effect. These experimental results show that the prepared SD with a structure of Au/(AgCdS:PVP)/n-Si has good photodiode behavior.

Similar reports have been reported in the literature [32–37]. Among them, B. Ezhilmaran et al. [34] studied the detection mechanism and evaluation parameters of Schottky-type photodetectors and the recent developments in this area achieved using various 2D materials in the past five years are reviewed. Emerging strategies to enhance the performance by adjusting the Schottky barrier height (SBH) are elaborated. X. Zhao et al. [35] present the impact of epitaxial quality, contact resistance, and profile of Ge PIN photodetectors (PDs) on dark current and responsivity. They were found as selectively grown PDs with Ge thickness of 500 nm, TDD was still low resulting in low dark currents. The dark current densities (at − 1 V) of non-selectively and selectively grown PDs with optimized profiles were measured to be 5 mA.cm^{-2} and 47 mA.cm^{-2}, respectively, while the responsivity of these detectors was 0.17 A.W^{-1} and 0.46 A.W^{-1} for $\lambda \cong 1.55 \times 10^{-4}$ cm, respectively so it has excellent performance for detection of this wavelength. Liming Wang et al. [36] show that after thermal treatment at an appropriate temperature, while the value of photocurrent increases, dark current decreases. That is, thermal treatment can improve the crystalline quality and enhance
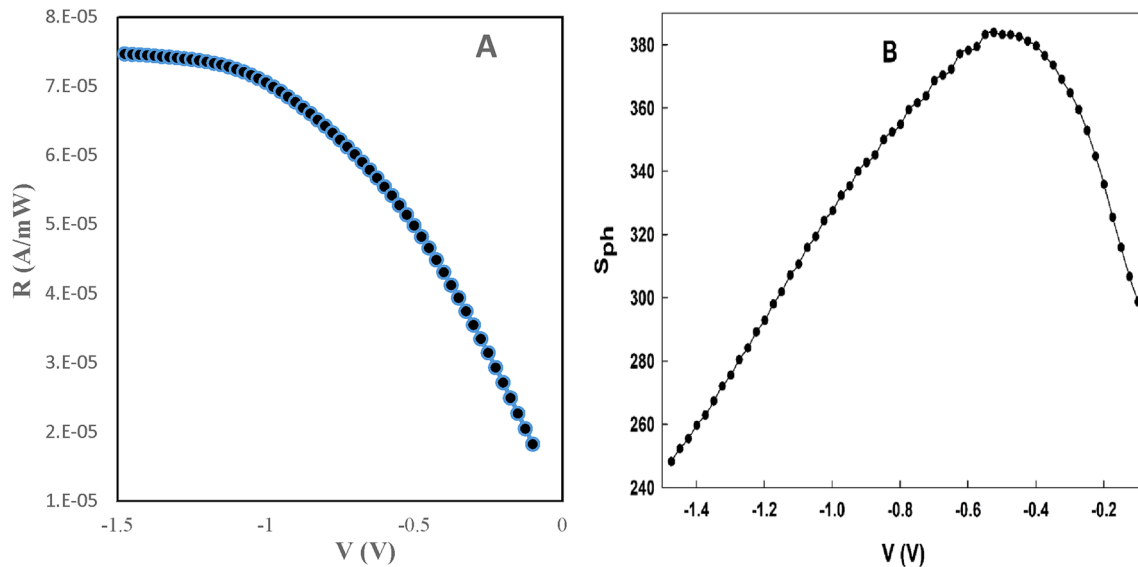
Fig. 7 The plots of **a** photoresponsivity and **b** photosensitivity depending on bias voltage for the produced SD under 100-Mw cm^{-2} illumination

the performance of optoelectronic devices based on GeSn alloy films. A Schottky diode was designed and formed as one of the contacts (based on NiSi(C)/TiW) to MQWs whereas on the other side, the structure had an Ohmic contact by M. Moeen et al. [37]. The thermal response of the detectors is expressed in terms of temperature coefficient of resistance (TCR) and the quality of the electrical signal is quantified by the signal-to-noise ratio. An excellent value of TCR $= -6\%/K$ and $K_{1/f} = 4.7 \times 10^{-14}$ were measured for the detectors which consist of the MQWs in series with the SD. These outstanding electrical results indicate a good opportunity to manufacture low-cost Si-based IR detectors soon.

3.2 The C/G–V characteristics of the fabricated SD

The capacitance (C) and conductance (G/ω) data were measured as a function of bias voltage at sufficiently low and high frequencies to obtain voltage-dependent profiles of N_{ss} and R_s. Figures 8 and 9 illustrate the plots of C and G/ω at the reverse and moderate/high forward bias regions corresponding to inversion, depletion, and accumulation regimes, respectively. The observed bending or narrow peak at the accumulation region is owing to the series resistance (R_s) and polymeric interlayer.
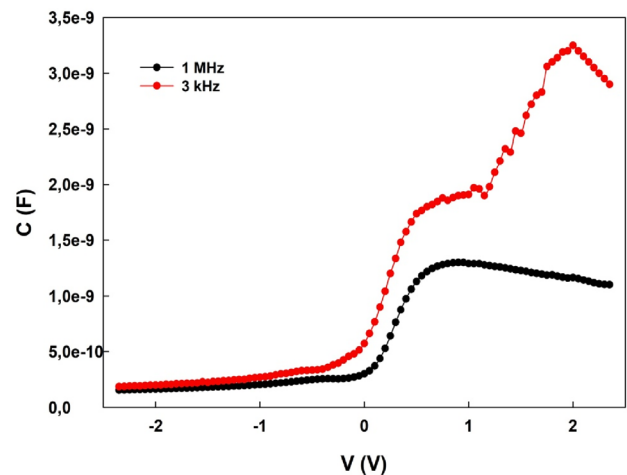

Fig. 8 The C–V plots of the manufactured SD in the dark and under a light intensity of 100 mW cm^{-2}

It should be mentioned that series resistance (R_s) and surface/interface state density (N_{ss}) are two crucial parameters, affecting the (C/G)–V and I–V characteristics. The R_s parameter becomes effective particularly at the accumulation region, resulting in a peak. However, the effect of N_{ss} is observed in the inversion and depletion regions. As seen in Figs. 8 and 9, the higher values of C and G/ω are obtained at a frequency of 3 kHz. The excess capacitance-conductance ($C_{ex} - G_{ex}/ω$)
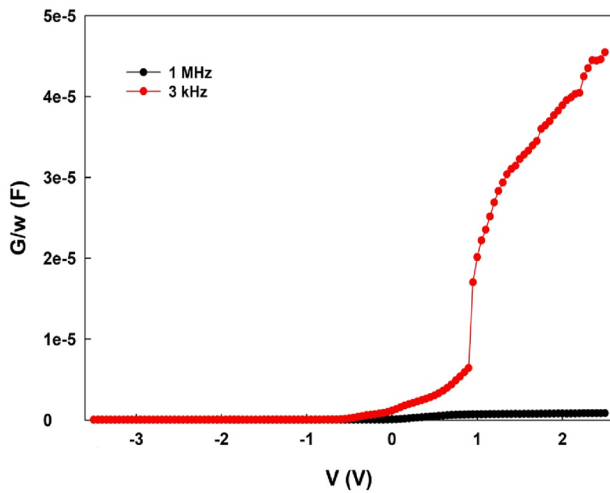
Fig. 9 The G/ω–V profiles of the prepared SD at dark and under an illumination intensity of 100 mW cm^{-2}

is demonstrated at low frequencies because of trapping the charge carriers. The increase in G/ω and the decrease in C at the accumulation region is known as "inductive behavior," originating from the series resistance (R_s) and the interfacial layer [1–5]. Based on the Nicollian & Brews [2–4], voltage-dependent R_i values can be computed at the considered frequencies as follows:

$$R_s(V) = \frac{G_{mi}}{\left[G_{mi}^2 + (\omega C_{mi})^2\right]} \tag{7}$$

As could be observed from Fig. 10, the R_s shows a decreasing behavior from the inversion region to the accumulation region, for which the real value of R_s can be obtained at a sufficiently high frequency (1 MHz). It becomes nearly voltage-independent at the accumulation region. On the other hand, the value of R_s needs to be utilized during the extraction of electric or dielectric parameters for these devices to eliminate its effect on the C–V and G–V curves, especially at high frequencies in the accumulation region. The depletion layer capacitance (C) per unit area of the MIS/MPS-type structure is given by [3]

$$C = \frac{|\partial Q_{SC}|}{\partial V} = \sqrt{\frac{q\varepsilon_s\varepsilon_0 N_D}{2\left(V_0 - V - \frac{kT}{q}\right)}} \tag{8a}$$

For the extraction of electrical parameters of the sample from the reverse bias C–V characteristics, Eq. (8a) should be arranged as follows:
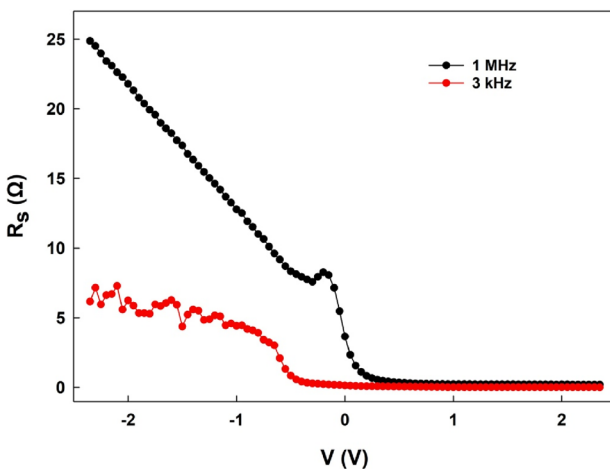

Fig. 10 The R_s–V profile of the fabricated SD at dark and under an illumination intensity of 100 mW cm^{-2} based on the Nicollian–Brews method
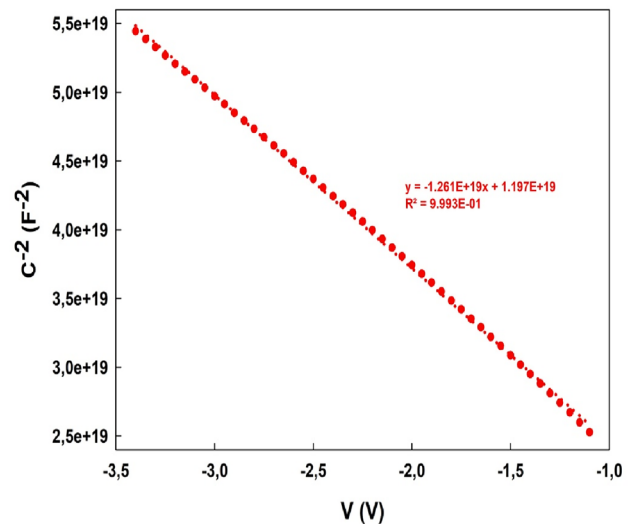

Fig. 11 The reverse bias C^{-2}–V curve of the fabricated SD at a frequency of 1 MHz

$$C^{-2} = \frac{2\left(V_0 - V - \frac{kT}{q}\right)}{q\varepsilon_s\varepsilon_0 N_D} \tag{8b}$$

Here, V_0 is the point where the C^{-2}–V plot intersects the C^{-2}-axis at zero bias so that the diffusion potential is obtained by

$$V_D = V_0 + kT/q \tag{9}$$

The density of donor atoms (N_D) can be determined using the slope of the C^{-2}–V graph (see Fig. 11) for sufficiently high frequencies as follows:

$$N_D = \frac{2}{q\varepsilon_s\varepsilon_0 A^2\left(\frac{dC^{-2}}{dV}\right)} \tag{10}$$

According to the intercept point (V_0) and slope of the C^{-2}–V diagram introduced in Fig. 11, the maximum electric field (E_m), the width of the depletion layer (W_D), Fermi level energy (E_F) at the M/S interface, and Φ_B(C–V) values were, respectively, obtained as follows [3, 4]:

$$E_m = \sqrt{\frac{2qN_D}{\varepsilon_s\varepsilon_0}}, \; W_D = \sqrt{\frac{2\varepsilon_s\varepsilon_0 V_0}{qN_D}}, \; E_F = \left(\frac{kT}{q}\right)\mathrm{Ln}\left(\frac{N_c}{N_D}\right), \text{ and } \Phi_{B(C-V)} = V_0 + \frac{kT}{q} + E_F \tag{11}$$

Thus, the value of V_0, N_D, E_F, W_D, E_m, and Φ_B(C–V) was found to be 0.949 V, 1.54×10^{16} cm^{-3}, 0.188 eV, 2.84×10^{-5} cm, 6.87×10^4 V cm^{-1}, and 1.162 eV, respectively. The BH value extracted from the C^{-2}–V curve, i.e., Φ_B(C–V), is more than the value extracted from the ln(I)–V curve, i.e., Φ_{B0}(I–V). Such a difference between Φ_{B0}(I–V) and Φ_B(C–V) could be associated with the nature of the measurement or calculation technique. It needs to be noted that the barrier that the charge carriers encounter from the semiconductor to the metal is always by a measure of E_F smaller than the barrier that they encounter from the metal to the semiconductor.

Another way to obtain voltage-dependent N_{ss} is to use the high-low-frequency capacitance ($C_{HF} - C_{LF}$) technique which is given by [3]

$$qAN_{ss} = \left[\left(\frac{1}{C_{LF}} - \frac{1}{C_i}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_i}\right)^{-1}\right] \tag{12}$$

Here, C_i is the interlayer capacitance, C_{LF} denotes the capacitance at low frequency, C_{HF} refers to the capacitance at high frequency, and A is the Schottky
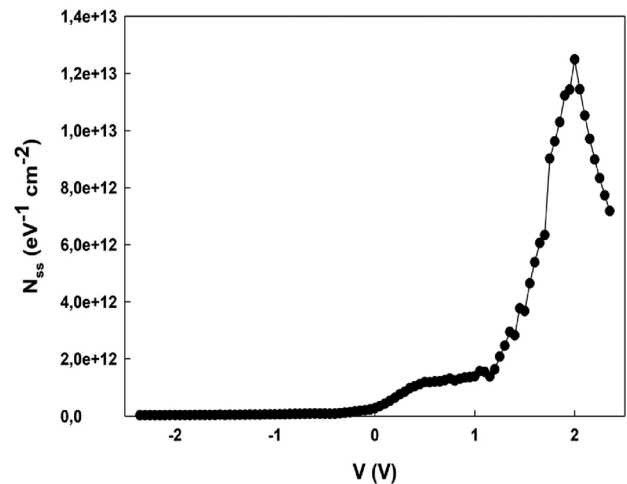

Fig. 12 The N_{ss}–V curve of the constructed SD obtained from the high-low-frequency capacitance method

contact area. Figure 12 demonstrates the voltage-dependent profile of N_{ss} at a frequency of 1 MHz. As seen, the N_{ss} curve has a distinctive peak at a bias voltage of ~ 2 V because of the spatial distribution of surface states/traps in the forbidden bandgap of the semiconductor. Compared with the conductance method, the high-low-frequency capacitance technique is easier, quickly applicable, and preferable due to accurate results. Similar experimental findings were reported in the literature on the electrical parameters and surface states obtained from I–V and C/G–V measurements [30, 38–44].

4 Conclusion

In this study, an MPS-type SD with a structure of Au/(AgCdS:PVP)/n-Si was constructed and its mean electric factors were investigated by measuring I–V and C/G-V data in the reverse and forward bias regions at dark and under illumination. First, the basic electrical parameters such as n, I_0, Φ_B(I–V), R_s, and R_{sh} were obtained from the I–V curves according to the TE theory, Cheung functions, and Norde model. The energy-dependent plots of N_{ss} were driven utilizing the voltage-dependent n and Φ_B values. In addition, the CMs into the manufactured

SD was examined at the forward bias voltages. Next, the S_{ph} and R values under an illumination intensity of 100 mW cm^{-2} were found to be 384 and 7.50 A mW^{-1}, respectively. Such high photosensitivity and photoresponsivity under a light intensity of 100 mW cm^{-2} implies a good photodiode behavior of the fabricated Au/(AgCdS:PVP)/n-Si MPS-type SD.

Then, the voltage-dependent capacitance and conductance of the fabricated SD were measured at sufficient low and high frequencies. Moreover, the values of N_d, Φ_B(C–V), and W_d were extracted from the C^{-2}–V curve at a frequency of 1 MHz. The (C_{HF}–C_{LF}) method was also used for exploring the voltage dependence of surface states/traps density (N_{ss}). The maximum value of the N_{ss}–V plot was attributed to the spatial distribution of surface states/traps in the semiconductor's forbidden bandgap. Based on the experimental results, the Au/(AgCdS:PVP)/n-Si MPS-type SD could be a candidate for electronic and optoelectronic applications instead of conventional MS-type SDs considering the advantages of polymers such as high mechanical strength, flexibility, low weight, inexpensive, and easy production processes.

Author contributions

The author's contribution to this article is as follows: G. Aslanbaş contributed to Conceptualization, Experiments, Formal analysis, Discussion, and Writing—original draft; P. Durmuş contributed to Investigation, Supervision, and Writing—review and editing; Ş. Altındal contributed to Supervision and Writing—review and editing; Y. Azizian-Kalandaragh contributed to Methodology, Supervision, Project administration, and Writing—review and editing.

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Data availability

The data are available from the corresponding author upon reasonable request.

Declarations

Conflict of interest   The authors declare that they have no conflict of interest.

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