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ORIGINAL RESEARCH ARTICLE

Effect of TiO_2-Surfactant Interface on the Electrical and Dielectric Properties of a Metal–Insulator–Semiconductor (MIS) Structure

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Abstract

To explore the effect of a TiO_2-surfactant (Brij 58) insulator as an interfacial layer on the electrical properties of a metal–semiconductor (MS) structure, a Au/TiO_2-surfactant/n-Si (MIS) structure was created on an n-Si wafer. The spin coating method was used to deposit a TiO_2 layer on the Si wafer. The electrical performance of the MIS structure is of great importance, and its study at forward and reverse biases requires the use of the *I–V* data (from −4.5 V to +4.5 V). The values of the reverse saturation current (I_0), series resistance (R_s), shunt resistance (R_{sh}), and rectification ratio (RR) are this structure's essential electrical characteristics that are calculated and compared with those of the MS structure. By measuring the energy dependence at forward bias, the density distribution of the surface states can be ascertained. The current conduction mechanisms are also determined. Moreover, the dielectric features of the MIS structure are extensively studied by calculating the values of ε', ε'', tanδ, R_s, and σ over a range of bias voltages (0.25–4 V) and frequencies (1 kHz–1 MHz) using $C/(G/\omega)$–V and $C/(G/\omega)$–f measurements. The C^{-2}–V plot of the structure is examined at a frequency range of 1 kHz–1 MHz. The results of these measurements are discussed in detail, providing insight into the changes in the impedance properties of the MIS device.

Keywords Schottky barrier structure · TiO_2-surfactant insulator interlayer · electrical and impedance properties

Introduction

Metal–semiconductor (MS) structures with/without an interlayer are necessary to efficiently operate electronic and optoelectronic devices such as solar cells (SC), Schottky diodes (SDs), transistors, and photodiodes. These instruments are not able to reach their full potential without MS structures.[1,2] Thanks to the versatility of MS structures, they can be employed for both rectifying and non-rectifying applications. The design of metal–insulator/polymer–semiconductor (MIS/MPS) structures has garnered increasing attention in recent times, offering a way to regulate and increase the potential barrier height (BH), as well as enhancing the electrical and dielectric performance of MS structures.[3] When a layer of oxide or insulator is situated between the metal and semiconductor layers, MIS structures are formed. These structures offer a viable alternative to MS-type SDs in electronic and optoelectronic devices, significantly improving performance by modulating the critical parameters including series resistance (R_s) and interface states (N_{ss}).[4] The presence of an interfacial layer at the M/S interface not only modifies the electrical properties of the MS structure, but also significantly affects the capacitance (C) and conductance (G/ω) of the MS device. These changes in response to the voltage and frequency are caused by the changes in the R_s, as well as interface traps or N_{ss} distribution at the M/S interface. The N_{ss} and polarization effects play the main role

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in the depletion region at lower frequencies, while the R_s and interfacial layer become more influential in the accumulation region at higher frequencies.[5] Therefore, the electrical and dielectric performance of these structures is determined by the R_s, the distribution of N_{ss}, material, thickness, and permittivity of the interlayer employed.

It must be noted that the fabrication procedure of MIS-type SDs is heavily dependent on the creation of pristine Si surfaces and the deposition of the insulator or oxide on this surface, which can have a major impact on the stability and reliability of the device.[1] The growing significance of these devices is due to their extensive range of optoelectronic and high-frequency uses. MIS diodes have a thin insulator layer at the M/S interface; this insulator layer prevents the inter-diffusion between the metal and the semiconductor substrate, and it can also solve the electric field reduction issue in MIS-type SDs.[6] The insulator layer causes a capacitor property in the MIS-type SDs, enabling it to store electric charges owing to the dielectric substance of the oxide layers. Nevertheless, traditional oxidation or deposition techniques for forming an insulator layer on Si substrate cannot completely passivate the active dangling bonds at the semiconductor surface. Furthermore, oxygen ions can create space charge impacts at low frequencies that are highly pronounced.[7]

Recently, alternative high-κ materials such as ZnO, HfO_2, ZrO_2, Si_3N_4, Al_2O_3, SiO_2, and TiO_2 have been gaining considerable attention for their potential use as interfacial insulator layers at M/S interfaces in semiconductor devices such as MIS.[8] Bulk TiO_2 is a promising option among these high-κ materials due to its various phases that boast an extraordinarily high dielectric constant. The MS structures with metal oxide interlayers are typically used in the fabrication of basic electronic devices such as diodes, photodiodes, collar cells, transistors, and capacitors depending on interlayer thickness and front semi-transparent metal rectifier contacts. They are also essential for space applications, as they can withstand harsh atmospheric environments with strong ionization radiation fields and high-temperature atmospheres. In particular, the high-κ dielectric interlayer offers enhanced capacitance, high energy storage capability and breakdown voltage, and low leakage current. Therefore, they may have the potential to replace conventional SiO_2 in the future.

Titanium, the world's fourth most abundant metal and the ninth most abundant element, was discovered in 1791 in England by Reverend William Gregor. It may be generally found in many minerals such as rutile, ilmenite, leucoxene, anatase, brookite, perovskite, sphene, titanates, and many iron ores. Rutile contains 93–96% TiO_2, ilmenite contains 44–70% TiO_2, and leucoxene contains up to 90% TiO_2.[4] The dielectric constant of the TiO_2 insulator or metal oxide varies between 16 and > 100.[4] TiO_2 has good chemical stability, non-toxicity, low cost, and a high refractive index. Thus, it is used as an anti-reflection coating material in solar cells and optical thin film devices. Despite all this, it is important to compare the prepared samples with similar ones and to accurately determine their repeatability, shortcomings, and advantages. For example, TiO_2 may be crystallized in different crystallographic polymorph phases such as anatase, rutile, and brookite. The most popular ones are the anatase and rutile phases; the first is typically formed at low temperatures while the second is thermodynamically stable at high temperatures.[4]

The formation process for the TiO_2 layer at the M–S interface, the annealing temperature, R_s, the inhomogeneous formation of the Schottky barrier at the M/S interface, and the distribution of N_{ss} at the Si/TiO_2 interface are the main factors determining the performance and reliability of TiO_2-based MIS structures.[9] A variety of methods can be used to grow thin films of TiO_2, including thermal or anodic oxidation, sol–gel technique, chemical vapor deposition, plasma-enhanced chemical vapor deposition, electron beam evaporation, and DC reactive magnetron sputtering.[10–12] However, the last method is the preferred choice for fabricating insulator films with consistent and desired properties, due to its ease of control. In recent years, many researchers have investigated MIS SDs due to their technological importance.[8–12] However, there are no detailed investigations on the electrical and dielectric properties as a function of applied voltage and frequency for MS structures with a high-dielectric TiO_2 interlayer.

Even if a metal oxide (MO), ferroelectric, or other thin interlayer is prepared under the same conditions, comparing its dielectric constant and electric modulus is not as easy as an electrical parameter. The dielectric properties of an MIS structure depend on many factors. Among these, the thickness, homogeneity, preparation temperature, and method are the most influential parameters of dielectric features, as well as the voltage, frequency, and temperature.[4,14–16] Since the MIS structure has sufficiently high R_s and N_{ss}, the dielectric parameters become a strong function of applied frequency and voltage. The changes in the real/imaginary components (ε', ε'') of a complex dielectric (ε^*) are quite significant, especially in the inverse and accumulation regions at low/moderate frequencies due to the surface/interface density of states (N_{ss}) and polarization processes. However, the R_s and interlayer are influential only at the accumulation region at higher frequencies.

This study aims to investigate both the electrical and dielectric features of an MS-type SD with a TiO_2-surfactant interlayer at the interface of the MS structure, with a view to its potential use in electronic applications, by measuring the *I–V*, $C/(G/\omega)$–*V*, and $C/(G/\omega)$–*f* characteristics. For this purpose, an MS-type SD with a Au/TiO_2-surfactant/n-Si structure is fabricated on a Si wafer, as described in the following section. The *I–V*

characteristics of the structure are measured from −4.5 V to 4.5 V, and the TE, Norde, and Cheung methods are used to calculate the electrical parameters including I_0, n, BH, R_{sh}, and R_s. Also, the Card–Rhoderick method is employed to extract the N_{ss} profile as a function of energy in the forward bias voltage. Next, the mechanisms of current conduction or transfer in the Au/TiO_2/n-Si structure are characterized at the reverse and forward bias regions. Then, the impedance of the fabricated MIS structure as a function of applied voltage and frequency ($C/(G/\omega)$–V, $C/(G/\omega)$–f) is determined in the voltage range from 0.25 to 4 V and the frequency range from 1 kHz to 1 MHz to obtain the ε', ε'', tanδ, R_s, and σ parameters. The profile of C^{-2}–V for the MIS structure is also investigated in the frequency range from 1 kHz to 1 MHz. Finally, a detailed discussion is provided on the obtained results.

Materials and Methods

Synthesis of TiO_2-surfactant Insulator

A sol–gel solution was prepared as follows. First, 0.512 g of Brij 58 surfactant was dissolved in EtOH, with stirring for 10 min. The obtained solution was then added to pure $TiCl_4$ (1 ml) and the mixture was stirred for 5 min. H_2O (1.642 g dropwise) was then added to the mixture, and the final solution was stirred at room temperature for 15 min before spin coating. The molar ratio of the final solution ($TiCl_4$:Brij 58:EtOH:H_2O) was 1:0.05:40:10.[13] The prepared solution was spin-coated on the substrate at 2000 rpm for 1 min, resulting in a sol–gel composed of surfactant tubular micelles with a diameter of 3–4 nm, surrounded by the titania precursor in a cubic order. The underside of the Si wafer was coated with a 100-nm-thick Al layer by sputtering at a pressure of 1.33×10^{-7} kPa, followed by annealing at 500°C to form a low-resistivity ohmic contact. After that, the TiO_2 layer was coated onto an n-Si wafer with 300 µm thickness and 1–10 $\Omega\cdot cm^{-1}$ resistance, utilizing the spin coating method. Finally, an MIS-type SD was prepared by using masks with 1.2 mm diameter and 100 nm thickness and placing Schottky or rectifier contacts with a tablet form on the TiO_2-surfactant insulator layer. This was accomplished through an MIS contact of Au/TiO_2/n-Si. To perform impedance (C/G–V) and I–V measurements, the prepared structures were fixed on a copper holder with the help of a conductive silver plate. Electrical contacts were made of silver-plated copper wires. The impedance and current measurements were performed utilizing an Agilent/Keysight HP4192A LF impedance analyzer and a Keithley 2400 source meter at room temperature, respectively.

Results and Discussion

Current–Voltage (I–V) Characteristics

Thermionic Emission (TE) Method

The TE theory is applied to obtain the main electrical parameters of MS- and MIS-type structures based on the I–V data in the forward bias region. This theory assumes that electrons and holes possess sufficient thermal energy to overcome the BH and be transferred.[14] If an MS or MIS structure has a large enough R_s and an ideality factor (n) greater than unity ($n=1$ in an ideal case), the I–V relationship is not like that of an ideal diode and deviates significantly from linearity (see Fig. 1a). In addition, the presence of a native interlayer or interlayer deposited onto the semiconductor surface, N_{ss}, between the interlayer and semiconductor also influences the I–V relation in the forward bias region. Thus, according to TE theory, the I–V relationship in these structures for $V>3$ kT/q can be defined as follows:[15]

$$I=\underbrace{AA^*T^2\exp\left(-\frac{q}{kT}\Phi_{B0}\right)}_{I_0}\left[\exp\left(\frac{q\left(V-IR_s\right)}{nkT}\right)-1\right], \tag{1}$$

where I_0 is the reverse saturation current, A^* refers to the effective Richardson constant, andΦ_{B0} and T are the zero-bias BH and temperature (K), respectively. The literature presents the other parameters well.[15–17] The intercept of the Ln(I)–V graph at an applied voltage of 0 V gives the value of I_0y (see the inset of Fig. 1a), and then the BH parameter, Φ_{B0}, can be computed by considering the rectifier contact area as follows:[2,15]

$$\Phi_{B0}=\frac{kT}{q}\mathrm{Ln}\left(\frac{AA^*T^2}{I_0}\right). \tag{2}$$

The values of I_0 and Φ_{B0} parameters were obtained as 2.27×10^{-8} A and 0.782 eV for the MS device and 4.59×10^{-9} A and 0.798 eV for the MIS device. The value of n is a key indicator of the effectiveness of MS/MIS-type structures, and ideally, it should be equal to 1. However, in the application, the value of n determined from the Ln(I)–V plot is often higher than 1 because of the presence of interlayers, its thickness (δ_i), N_{ss}, dielectric value, barrier inhomogeneity, and the width of the depletion layer (W_D) or doping level of acceptor or donor atoms in the semiconductor:[2,17]

$$n=\frac{q}{kT}\left(\frac{dV}{d(\mathrm{Ln}(I))}\right)=1+\left(\frac{\delta_i}{\varepsilon_i}\right)\left\{\frac{\varepsilon_s}{W_D}+qN_{ss}\right\}. \tag{3}$$

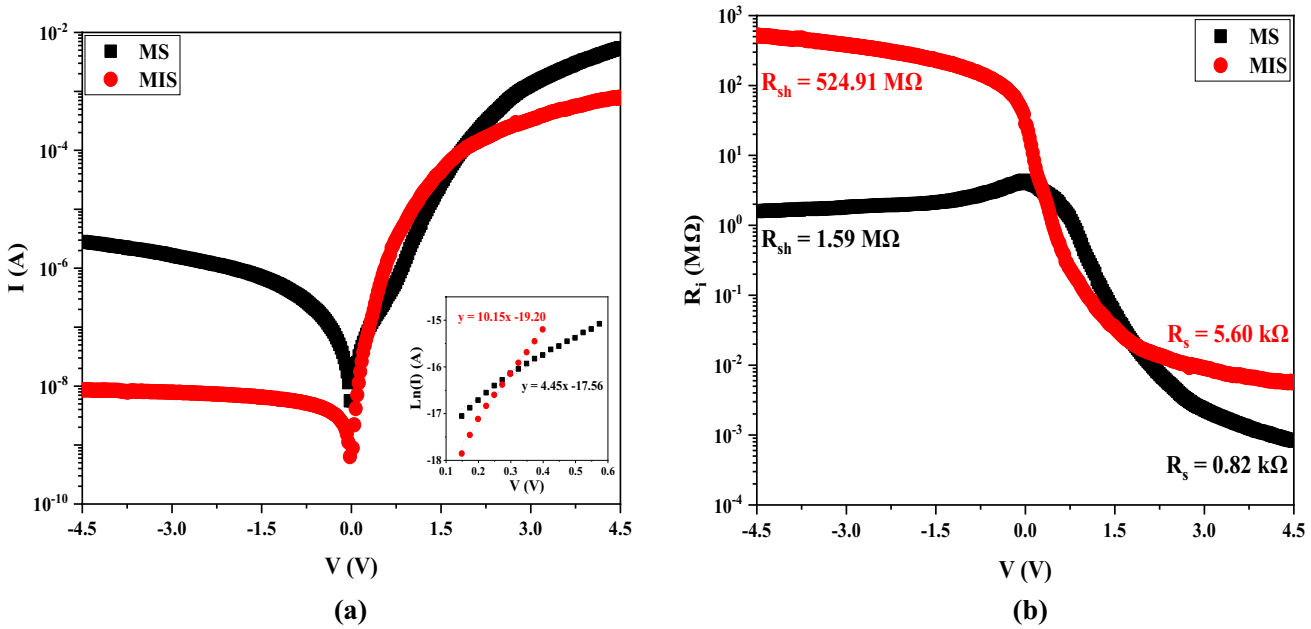

Fig. 1 Semi-logarithmic changes in (a) *I*–*V* and (b) R_i–*V* curves for the MS/MIS-type SDs.

The value of *n* for the MS and MIS structures was 8.59 and 3.81, respectively. To determine the resistance of the MIS structure at different applied voltage, Ohm's law ($R_j = dV_j/dI_j$) should be employed.[18] The resistance corresponds to the series and shunt resistance at the forward and reverse bias voltage, respectively. As can be observed in Fig. 1b, the R_s value is 0.82 kΩ and 5.60 kΩ at a forward bias voltage of 4.5 V, and the value of R_{sh} is 1.59 MΩ and 524.91 MΩ at a reverse bias voltage of −4.5 V for the MS and MIS structures, respectively. The primary parameter that determines the performance of the MS and MIS structures is the rectification ratio ($RR = I_F/I_R$), equaling 1.93×10^4 and 9.40×10^4, respectively.

Cheung Functions

The Cheung functions can be used to compute the fundamental electrical parameters of MS and MIS structures such as *n*, Φ_{B0}, and R_s when the forward bias voltage is high. This corresponds to the concave curvature of the Ln(*I*)–*V* curve, and can be accomplished utilizing the following relations:[19,20]

$$\frac{dV}{d(\mathrm{Ln}(I))} = IR_s + \left(\frac{nkT}{q}\right), \tag{4}$$

$$H(I) = V - \frac{nkT}{q}\mathrm{Ln}\left(\frac{I}{AA^*T^2}\right) = IR_s + n\Phi_B. \tag{5}$$

In general, the influence of the native deposited interlayer at the M/S interface and R_s leads to a decrease in the linearity of the Ln(*I*)–*V* curve at the forward bias region. The Cheung functions have a linear component in this area, enabling us to obtain R_s and *n* values with the slope and intercept of the d*V*/d(Ln(*I*))–*I* graph by Eq. 4. Moreover, the slope and intercept of the *H*(*I*)–*I* graph using Eq. 5 yield the second-Φ_{B0} and R_s values. As a result, the values of Φ_{B0}, *n*, and R_s were determined by the slopes and intercepts presented in Fig. 2 and are introduced in Table I.

Modified Norde Function

As another method, the use of the Norde function, *F*(*V*), enables the values of R_s and Φ_{B0} to be determined for the MIS structure. The Norde function is given as follows[20]:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\left[\mathrm{Ln}\left(\frac{I(V)}{AA^*T^2}\right)\right], \tag{6}$$

where γ corresponds to an integer that must be greater than *n*. Figure 3a shows the changes in *F*(*V*) for the prepared MS and MIS structures as a function of the applied bias voltage. The presence of a minimum point at the concave part of the *F*(*V*) function enables us to obtain the R_s and Φ_{B0} parameters with the Norde technique,[20] whose values are given in Table I.

The non-ideal behavior of the MIS structure is largely related to the N_{ss}. By analyzing the *I*–*V* data at the forward bias voltage, the N_{ss} profile in terms of energy can be

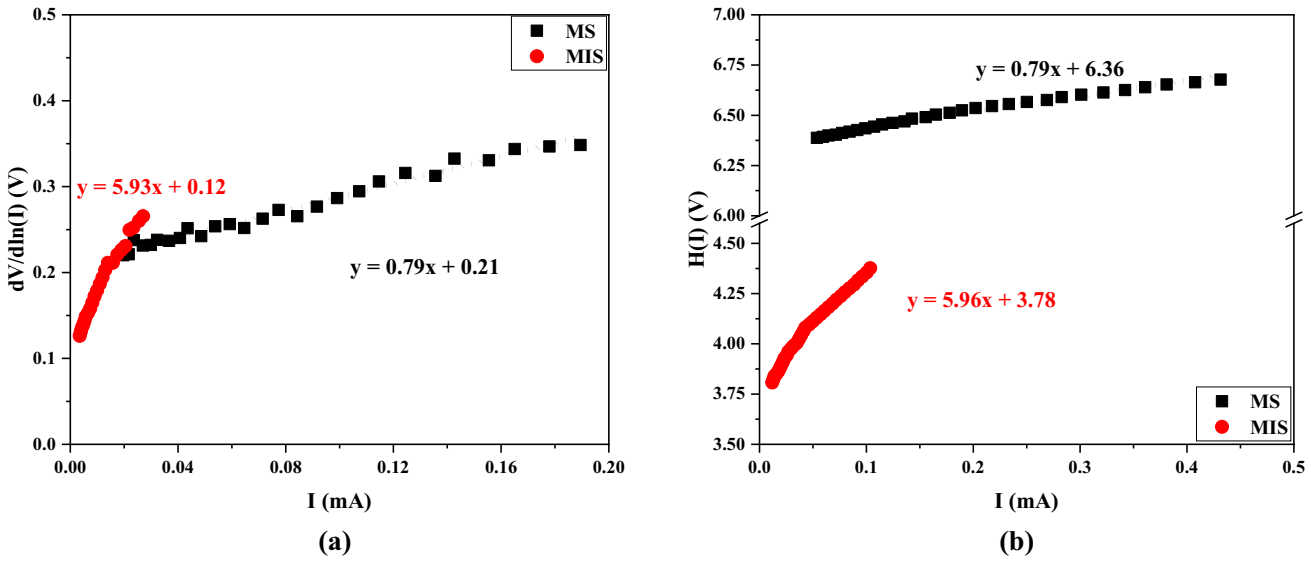

Fig. 2 Plots of (a) d*V*/d(Ln(*I*)) and (b) *H*(*I*) of the MS/MIS-type SDs.

Table I Electrical variables of the MS/MIS-type SDs obtained by different methods

Diode	Φ_{B0} (eV)			RR × 10^4	R_s (kΩ)				R_{sh} (MΩ)	n		N_{ss} ($eV^{-1}.cm^{-2}$) × 10^{14}	
	TE	Norde	*H*(*I*)		TE	Norde	*H*(*I*)	d*V*/dln(I)		TE	d*V*/dln(*I*)	TE	Norde
MS	0.78	0.83	0.79	1.93	0.82	0.81	0.79	0.79	1.59	8.59	8.08	0.42	0.35
MIS	0.80	0.80	0.80	9.40	5.60	6.14	5.96	5.93	524.91	3.81	4.62	1.32	0.29

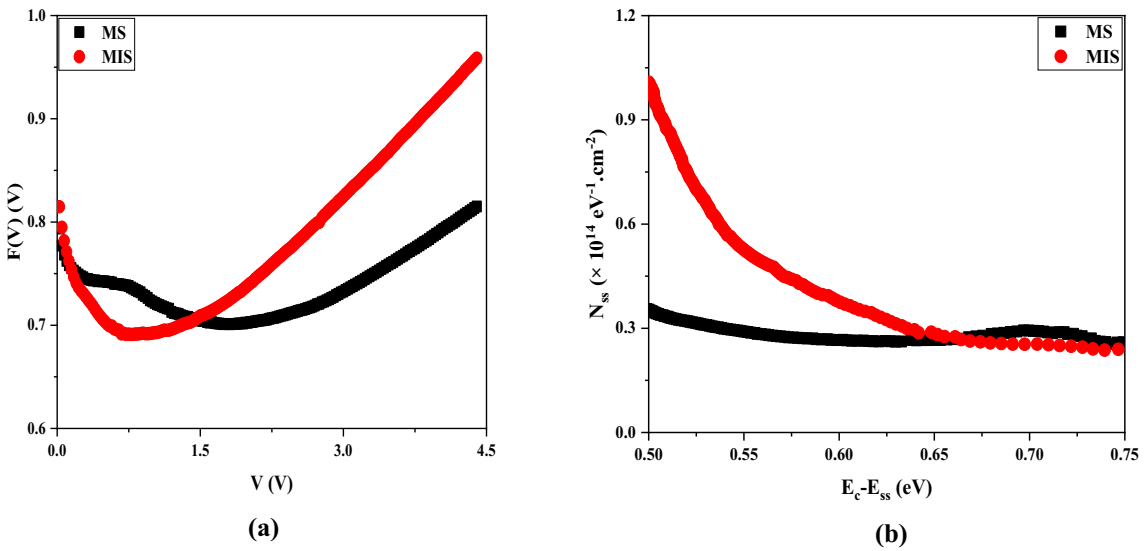

Fig. 3 Functions of (a) *F*(*V*) versus voltage and (b) N_{ss} versus energy for the MS/MIS-type SDs.

determined, taking into account both the voltage-dependent *n* and BH. At equilibrium, the values of N_{ss} can be extracted as follows:[2,13]

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V)-1) - \frac{\varepsilon_s}{W_D}\right], \quad (7)$$

where δ (=100 nm) and W_D (=0.0113 cm^2) are the interlayer thickness and the width of the depletion layer, and ε_i and ε_s are the interfacial layer and semiconductor permittivity, respectively. The difference in energy between the conduction band edge (E_c) and the N_{ss} level (E_{ss}) of an *n*-type semiconductor is defined by $E_c - E_{ss} = q(\Phi_e - V)$.[2,14]

Figure 3b illustrates the energy-dependent changes in the N_{ss} curve for the MS and MIS structures at room temperature. At 0.50 eV, the value of N_{ss} for both structures is extreme, whereas it gradually decreases with increasing energy, and finally, it reaches the minimum at 0.75 eV. It must be noted that the value of N_{ss} for the MIS structure is smaller than that for the MS structure at higher energies due to an insulator layer at the interface of M/S, which effectively passivates the semiconductor surface.[2,21]

Table I presents the basic electrical parameters for the MS and MIS structures which have been calculated by the TE theory and Norde and Cheung techniques. As can be seen in Table I, there are some discrepancies between electrical parameters obtained by the different approaches. These discrepancies are a result of voltage-dependent parameters and the nature of the calculation methods corresponding to the different bias voltages.

Current-Transport/Conduction Mechanisms (CTMs/CCMs)

The TiO_2-surfactant interfacial layer at the M/S interface influences the CCMs in the MIS structure at the forward and reverse bias voltage. Generally, the charge transport is significantly enhanced if deep traps or surface states occur at the interface of the M/S. Figure 4a presents the Ln(I_F) plot in terms of the applied voltage at the forward bias region for the MS and MIS structures, which consists of three linear parts corresponding to various CCMs. The slope of these linear regions equals 1.23, 5.86, 3.44 for the MS structure and 1.53, 3.69, 2.44 for the MIS structure. Ohmic behavior (I~V) is seen in the first part, with the bias voltage being relatively low. This is because a small electric charge is perfused into the semiconductor by the electrodes.[22] The slope of the other linear parts is higher than 2, indicating that the electric current is exponentially altered ($I \sim \exp(V^m)$). This is because the primary charge carrier process in these linear regions is recombination-tunneling.[23] It should be mentioned that two CCMs can occur in the MS and MIS structures at the reverse bias voltage, either the Poole–Frenkel (PF) or Schottky emission (SE) mechanisms. Once the PFE mechanism dominates, the value of I_R is given as follows[23,24]:

$$I_R = I_0 \exp\left(\frac{\beta_{PF}}{kT}\sqrt{\frac{V}{d}}\right). \tag{8}$$

The value of I_R will be determined with the following relation providing that the SE mechanism is dominant.

$$I_R = AA^*T^2\exp\left(-\frac{\varphi_B}{kT}\right)\exp\left(\frac{\beta_{SC}}{kT}\sqrt{\frac{V}{d}}\right), \tag{9}$$

where β_{PF} and β_{SC} are the field lowering coefficients for the PFE and SE mechanisms, related to each other by $2\beta_{SC} = \beta_{PF}$.[24,25]

The changes in the Ln(I_R)–$V^{0.5}$ plots of the MS and MIS structures are depicted in Fig. 4b. As can be observed, the Ln(I_R)–$V^{0.5}$ graph for the MS and MIS structures has a linear form in the sufficiently high reverse bias region. The slope of these linear plots is employed to compute the field lowering coefficient, which was obtained as 4.43×10^{-6} $eV^{-1}m^{0.5}V^{0.5}$ for the MS structure and 3.04×10^{-5} $eV^{-1}m^{0.5}V^{0.5}$ for the

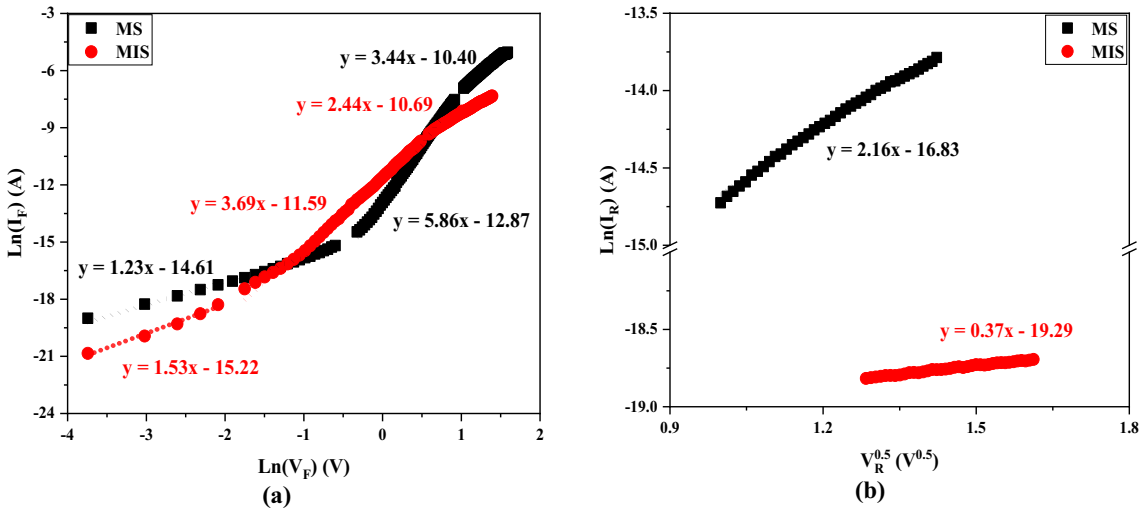

Fig. 4 Graphs of (a) Ln(I_F)–V_F and (b) Ln(I_R)–$V_R^{0.5}$ for the MS/MIS-type SDs.

MIS structure. By comparing the obtained experimental value and the theoretical result (3.79×10^{-5} $eV^{-1}m^{0.5}V^{0.5}$ for the MS structure and 5.96×10^{-6} $eV^{-1}m^{0.5}V^{0.5}$ for the MIS structure) of the β_{PF} coefficient, it is found that the PFE and SE mechanisms are the dominant CCMs in the MS and MIS structures, respectively.

Impedance Characteristics

Voltage Dependence of the Impedance

Figure 5 shows the *C–V* and *G/ω–V* curves of the prepared MIS structure at frequencies from 1 kHz to 1 MHz, measured at room temperature. As can be seen from Fig. 5a, the *C–V* and *G/ω–V* profiles of the fabricated MIS structure display similar inversion, depletion, and accumulation regions to those of the metal–oxide–semiconductor (MOS) structure. The *C–V* curves of the MIS structure in the frequency range from 1 to 1 MHz exhibit a local maximum in the depletion region; however, it can be increased or decreased by varying the applied bias voltage and frequency. This implies that the presence of an interfacial layer is capable of passivating active dangling bonds in the semiconductor crystal. Moreover, the presence of un-passivated N_{ss} and bulk traps enables the storage/capture and release/emission of many electric charges if a forward bias voltage is applied, thus resulting in an increase or decrease. Also, the *C–V* plots have a concave curvature in the accumulation part, originating from the R_s and the interlayer. This suggests that N_{ss} is particularly prominent in the depletion and inversion parts at low and moderate frequencies, while R_s and the interlayer are dominant in the accumulation part at higher frequencies.

In Fig. 5b, a distinct peak is seen in the *G/ω–V* profile near 0.75 V for the prepared MIS structure, which is caused by the unusual density of N_{ss} and dislocations between the insulator interlayer and the semiconductor at its forbidden energy level.[2,26]

The permittivity of SDs is a complex parameter ($\varepsilon^* = \varepsilon\prime - j\varepsilon''$) that has a major influence on their dielectric characteristics. The real part of this parameter is responsible for the amount of energy stored within the structure, which is given by

$$\varepsilon' = C/C_0 = Cd_i/\varepsilon_0 A. \tag{10}$$

The imaginary part of this parameter corresponds to the energy loss in the structure, which is defined as

$$\varepsilon'' = G/\omega C_0 = Gd_i/\varepsilon_0 \omega A, \tag{11}$$

where $C_0(=\varepsilon_0 A/d_i)$ is the geometric capacitance, A is the area of rectifier contact, ε_0 is the free space permittivity, and d_i is the interlayer thickness.[27] The changes in the ε' and ε'' parameters for the prepared MIS structure as a function of voltage in the frequency range of 1 kHz–1 MHz and room temperature are exhibited in Fig. 6a and b. It is evident that the values of ε' and ε'' vary significantly with the bias voltage and frequency, especially at the depletion and accumulation regions. The values of ε' and ε'' decrease with increasing frequency in these regions while remaining constant at the inversion region. It is noteworthy that the R_s of the MIS structure is the primary cause of such behavior of the ε′ and ε″ functions.[28] Also, the frequency-dependent ε′ and ε″ functions display a dispersion that is linked to Maxwell–Wagner and space-charge polarization.[29,30] The maximum value of

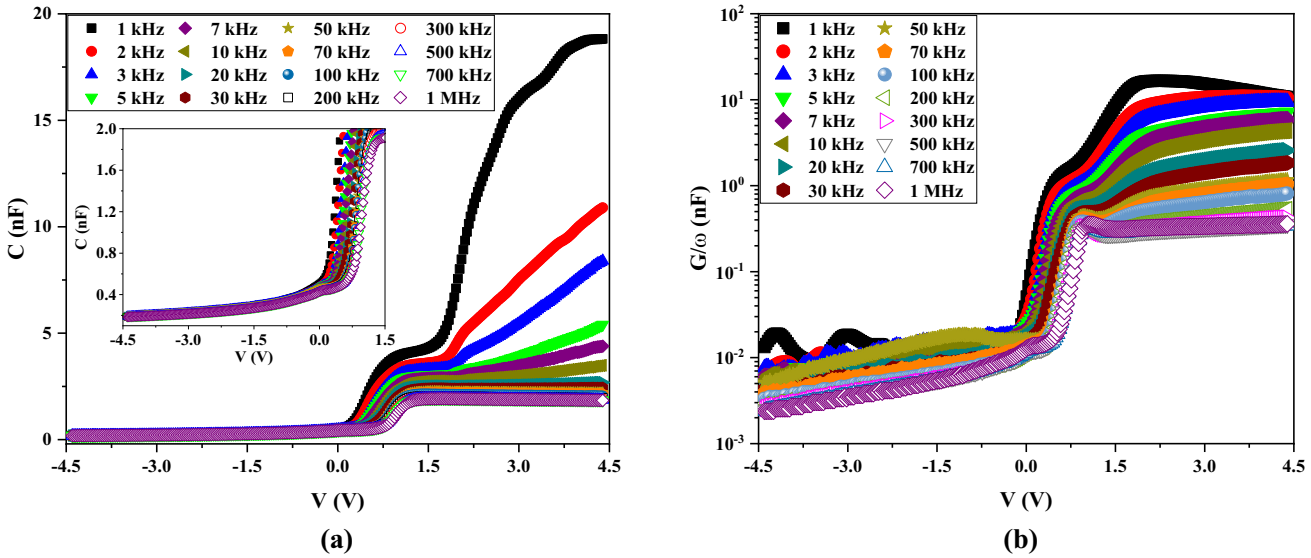

Fig. 5 Variations in (a) *C–V* and (b) *G/ω–V* for the MIS-type SD.

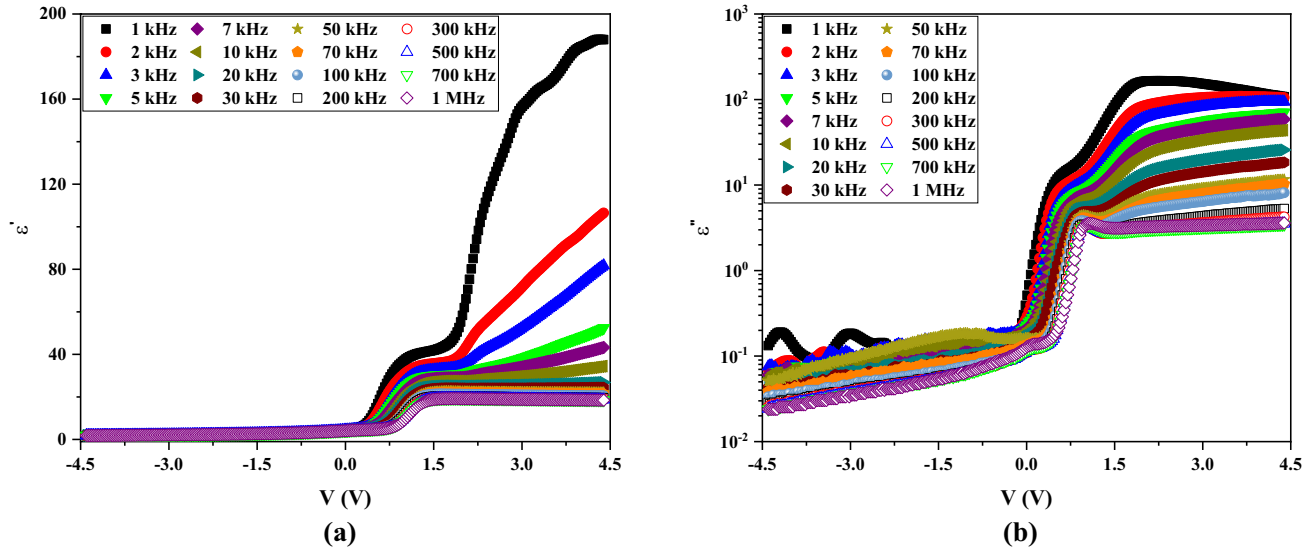

Fig. 6 Changes in (a) ε' and (b) ε'' functions in terms of voltage for the MIS structure.

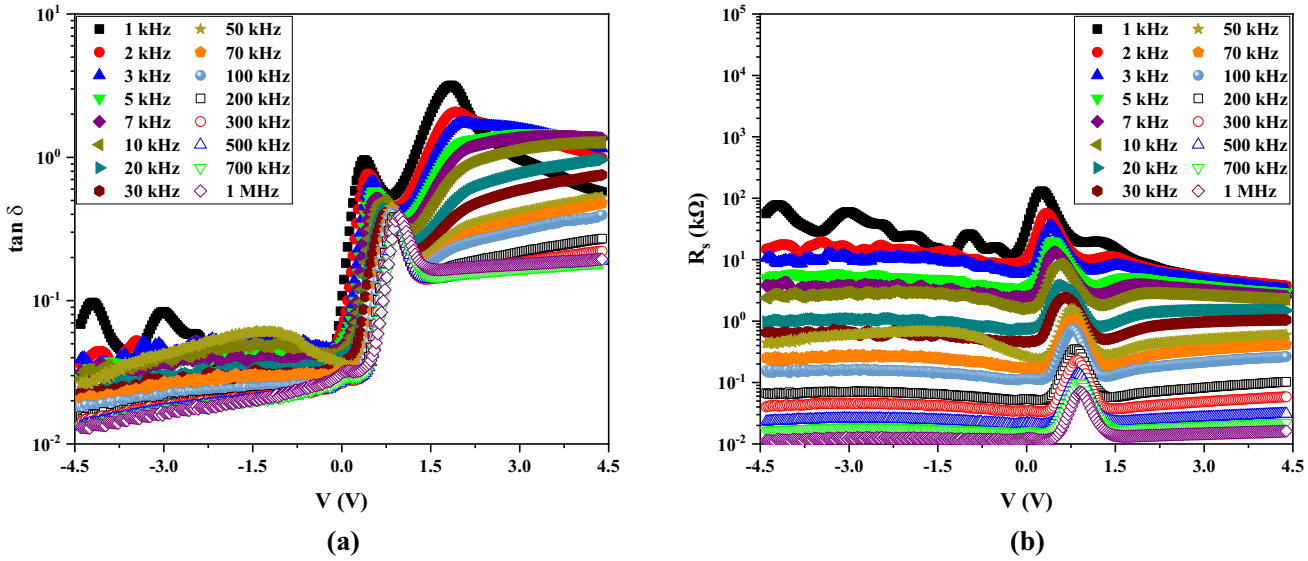

Fig. 7 Changes in (a) tanδ–V and (b) R_s–V profiles for the MIS-type SD.

ε' (=185) even at 1 kHz is almost 49 times that of the maximum dielectric value of conventional SiO_2. This means that the fabricated Au/TiO_2/n-Si structure has greater charge or energy capability when compared to other low-dielectric materials such as SiO_2 and SnO_2.

One of the fundamental electrophysiological factor of the MIS structure that requires study by considering the phase difference (δ) between the induced current and the applied electric field is the tangent loss (tanδ), which is indicated as follows.[27]

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} = \frac{G}{\omega C}. \tag{12}$$

Figure 7a demonstrates the changes in tanδ for the prepared MIS structure depending on the applied bias voltage over a frequency range from 1 kHz to 1 MHz. The value of tanδ for the MIS structure displays a peak at nearly all frequencies. The value of these peaks decreases as the frequency increases and the peak positions shift towards the negative-bias region. A variety of factors can influence the peak value of tanδ, including R_s, N_{ss}, surface or dipole polarization, and the thickness of the interlayer.[31] It is well known

that capacitance and conductance are highly responsive to the interfacial features because of the different behaviors of the N_{ss} at small and large frequencies.[32] Previous research has indicated that the appearance of the peak is likely caused by interface states.[33–35]

A high-dopant semiconductor material can reduce the BH at the M/S interface, leading to a decrease in the R_s of the MS device. The Nicollian and Brews method allows us to express the frequency-dependent R_s as[36]

$$R_s = \frac{G}{G^2 + (\omega C)^2}, \tag{13}$$

where C and G/ω refer to the measured capacitance and conductance of the device at the different applied bias voltages and frequencies. Figure 7b demonstrates the voltage-dependent profiles of R_s for the MIS structure in the frequency range of 1 kHz–1 MHz and at room temperature. As seen, the R_s value remains nearly constant at the accumulation part, which is in agreement with the actual value of R_s for the MIS structure. The R_s plots of the MIS structure demonstrate how the density of the N_{ss} between the interlayer and the semiconductor, as well as their relaxation times, affects the peak behavior at all frequencies.

The application of a bias voltage can lead to a restructuring and rearrangement of N_{ss}, which has an effect on the behavior of R_s. This effect is more pronounced at high frequencies and in the accumulation region, whereas it is negligible at low frequencies and in the inversion region.

It is necessary to compute the electrical modulus to assess the electrical conduction processes, describe the grains and grain boundary contributions, and eliminate the electrode polarization response in MIS structures. The real and imaginary components of the complex parameter ($M^* = M\prime - jM''$) are determined as follows[36–42]:

$$M' = \omega C_0 Z'' = \varepsilon'/(\varepsilon'^2 + \varepsilon''^2), \tag{14a}$$

$$M'' = \omega C_0 Z\prime = \varepsilon\varepsilon''/(\varepsilon'^2 + \varepsilon''^2). \tag{14b}$$

Figure 8a shows the evolution of the M' curves as a function of various applied voltages for frequencies between 1 kHz and 1 MHz at ambient temperature. It is obvious that the highest M' values across the whole frequency range are found at −4.5 V in the negative bias region, after which the values decrease with increasing applied voltage until they reach close to zero at +1.5 V. On the other hand, the monatomic dispersion caused by the short-range mobility of charge carriers causes the frequency to increase, thus increasing the value of M'.

Additionally, Fig. 8b shows the change in the voltage-dependent M'' profiles in the frequency range of 1 kHz to 1 MHz at ambient temperature. It is evident that the values of M'' close to 0.75 V are extreme and the peaks shift toward the negative bias region where the M'' values decrease with increasing the frequency. At applied voltages of −4.5 V and +4.5 V, the values of M'' are nearly constant.

The C–V measurements for the MIS sample are carried out using an AC voltage signal (V_{ac}) and an applied DC voltage, as shown in Fig. 5a. The N_{ss} can readily track the AC signal at lower frequencies while it lacks this capability at higher frequencies. Thus, the N_{ss} profile is calculated using the low (C_{LF})–high (C_{HF}) frequency capacitance approach as follows:[15,16]

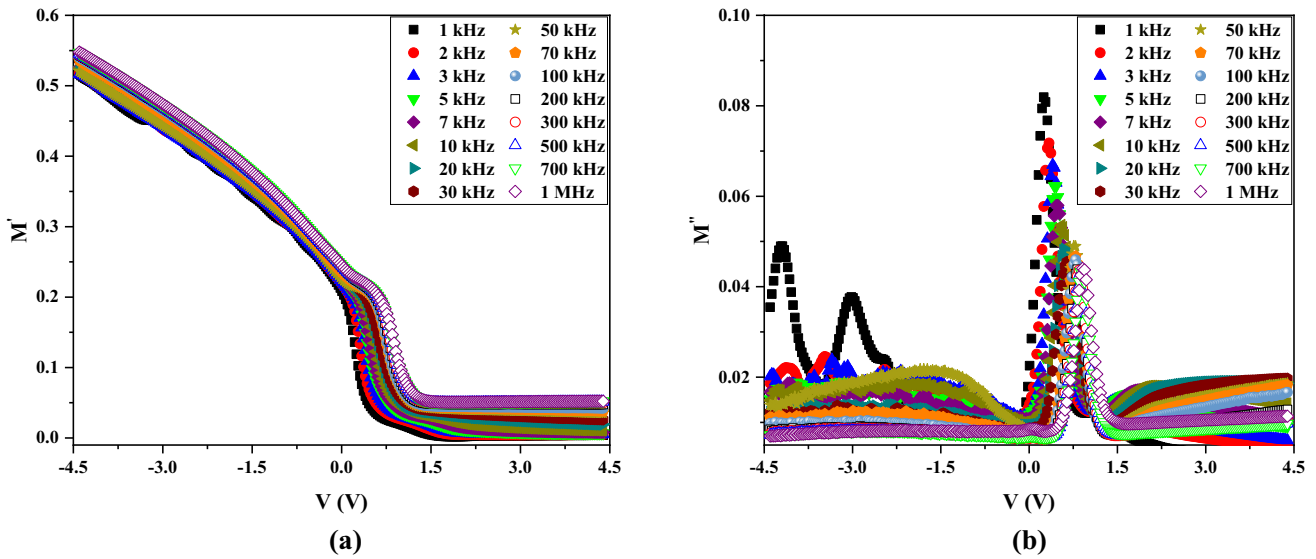

Fig. 8 Graphs of (a) M' and (b) M'' versus V for the MIS structure.

$$N_{ss} = \frac{1}{qA}\left[\left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1}\right]. \quad (15)$$

In Fig. 9a, the voltage-dependent N_{ss} profile is depicted. The MIS structure's N_{ss} profile has a maximum value of 8.84×10^{13} eV^{-1} cm^{-2} at 4.5 V applied voltage. However, it is nearly constant throughout the region of negative bias from −4.5 V to +0.5 V, at 2.21×10^{9} eV^{-1} cm^{-2}.

At the inversion region, the depletion layer capacitance of the fabricated MIS-type SD is determined as[1,43]

$$C^{-2} = \frac{2(V_d + V)}{qA^2\varepsilon_s N_D}, \quad (16)$$

where V denotes the bias voltage applied, q is the electric charge, A is the area of the MIS device, ε_s is the semiconductor permittivity, and N_D is the ionized trap–like donor. In addition, V_d refers to the diffusion potential at zero-bias voltage acquired with the intercept of the C^{-2}–V graph. The voltage-dependent C^{-2} illustrations of the fabricated MIS-type SD in the frequency range of 1 kHz–1 MHz at room temperature are presented in Fig. 9b. The profiles of C^{-2}–V for the MIS structure at different frequencies demonstrate a strong linear relationship between C^{-2} and the applied bias voltage from −2 V to −1 V, whose slopes increase slightly with the increase in frequency.

The C^{-2}–V profiles can be used to derive the primary electronic properties of the MIS structure, including N_D, width of the W_d, BH (Φ_B), and Fermi energy (E_F), at each applied frequency. Utilizing the intercept and slope of the C–V graph at each frequency, the intercept bias voltage (V_0) and N_D were computed. Additionally, the E_F and BH values of the MIS structure were calculated as follows[38]:

$$E_F = \frac{kT}{q}\ln\left(\frac{N_C}{N_D}\right), \quad (17)$$

$$\Phi_B = V_0 + kT/q + E_F - \Delta\Phi_B, \quad (18)$$

where kT/q refers to the thermal energy, N_C is the state-to-state density at the conduction band, and $\Delta\Phi_B$ denotes the image force lowering. In addition, W_d and N_D are calculated with the intercept voltage ($V_0 = V_D - kT/q$) and the slope ($\tan\theta$) as

$$W_d = (2\varepsilon_s\varepsilon_o V_D/qN_D)^{1/2}, \quad (19)$$

$$N_D = 2/(q\varepsilon_0\varepsilon_s A^2\tan\theta). \quad (20)$$

Table II presents the C–V measurement results for the electronic properties of the MIS structure in the frequency range of 1 kHz–1 MHz. A high intercept voltage is unavoidably caused by the insulator layer at the M/S interface, series resistance (R_s), and N_{ss}. Additionally, at higher frequencies, the value of R_s has a greater effect, whereas at lower frequencies, the N_{ss} factor is more important.[24,38]

The electrical conductivity of the Schottky structure as a function of frequency is described as follows:[34,35]

$$\sigma = \left(\frac{d_i}{A}\right)\omega C\tan\delta = \varepsilon_0\varepsilon''\omega. \quad (21)$$

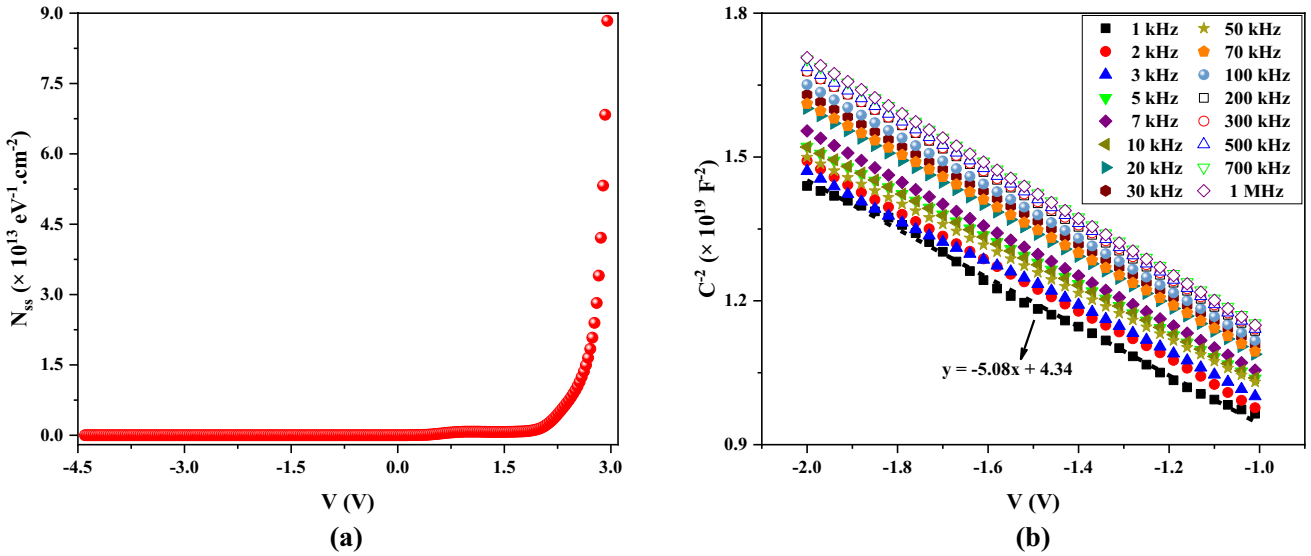

Fig. 9 Plots of (a) N_{ss}–V and (b) C^{-2}–V profiles for the MIS sample.

Table II Electronic parameters of the MIS sample obtained by *C–V* measurement

F (kHz)	V_o (V)	V_D (eV)	N_D ($\times 10^{16}$ cm^{-3})	E_F (eV)	E_m (kV/cm)	W_D (μm)	$\Delta\Phi_B$ ($\times 10^{-4}$ eV)	Φ_B (eV)
1	0.85	0.88	1.85	0.18	69.50	0.25	9.55	1.06
2	0.90	0.92	1.82	0.18	70.72	0.25	9.63	1.10
3	1.16	1.18	2.02	0.18	84.72	0.27	10.54	1.36
5	1.12	1.15	1.92	0.18	81.13	0.28	10.32	1.32
7	1.10	1.12	1.87	0.18	79.34	0.28	10.20	1.30
10	1.13	1.15	1.92	0.18	81.38	0.28	10.33	1.33
20	1.10	1.13	1.82	0.18	78.42	0.28	10.14	1.31
30	1.10	1.13	1.78	0.18	77.60	0.28	10.09	1.31
50	1.17	1.19	1.98	0.18	84.08	0.28	10.50	1.37
70	1.09	1.11	1.79	0.18	77.30	0.28	10.07	1.29
100	1.07	1.10	1.74	0.18	75.61	0.28	9.96	1.28
200	1.07	1.10	1.71	0.18	75.13	0.29	9.93	1.28
300	1.10	1.13	1.73	0.18	76.40	0.29	10.01	1.31
500	1.07	1.10	1.70	0.18	74.85	0.29	9.91	1.28
700	1.07	1.09	1.69	0.18	74.29	0.29	9.87	1.27
1000	1.03	1.06	1.67	0.18	72.62	0.29	9.76	1.24

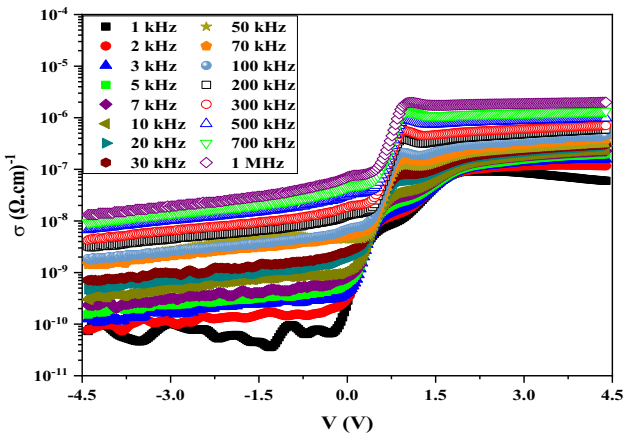

Fig. 10 Semi-logarithmic plots of *σ–V* for the MIS sample.

Figure 10 presents the graph of voltage-dependent σ for the prepared MIS structure in the frequency range of 1 kHz–1 MHz at room temperature. It is evident that the value of σ increases with increasing frequency, unlike the ε' and tanδ parameters. It is worth mentioning that the electrical conductivity, which is infinite at zero frequency and negligible at larger frequencies, directly influences the dielectric loss.[31] Moreover, the electrical conductivity increases with the increase in the bias voltage because of the reduced polarization, resulting in an increase in the eddy current and a consequent increase in the energy loss (tanδ).[29]

Frequency Dependence of the Impedance

The frequency-dependent capacitance and conductance of the prepared MIS structure were examined in the frequency range of 1 kHz–1 MHz at a bias voltage range of 1–2.5 V and 0.25–4 V, respectively. Figure 11a and b depict the changes in the capacitance and conductance of the MIS structure depending on the frequency at different applied bias voltages. When the frequency is increased, the dispersion effect prevents the charges at interface states and in equilibrium with the semiconductor from influencing the capacitance, resulting in the AC signal not being tracked.[37] Thus, the capacitance of the MIS structure exhibits an exponential variation with frequency. As the frequency increases, G/ω decreases because electrical dipole moments cannot effectively describe the electric field at higher frequencies.[38–40]

The changes in the frequency-dependent ε' in the bias voltage range of 0.25–4 V and frequency range of 1 kHz–1 MHz at room temperature are introduced in Fig. 12a. When the frequency reaches almost 100 kHz, the ε' profiles of the MIS structure are near their minimum values, and after this, they remain constant with the increase in the frequency. At lower frequencies, the energy stored in the MIS structure increases significantly provided that a higher bias voltage is applied. However, the stored energy is nearly constant at different bias voltages at higher frequencies. At these frequencies, the polarization decreases because N_{ss} is not able to maintain the AC signal and finally reach a constant value. This leads to a decrease in the value of ε', as the electrons are not able to follow the external field beyond a particular frequency.[35]

It is useful to study the frequency-dependent energy loss of the fabricated MIS structure by plotting the imaginary part of the complex permittivity (ε'') in the frequency range of 1 kHz–1 MHz at different bias voltages and room temperature, as shown in Fig. 12b. The energy loss of the

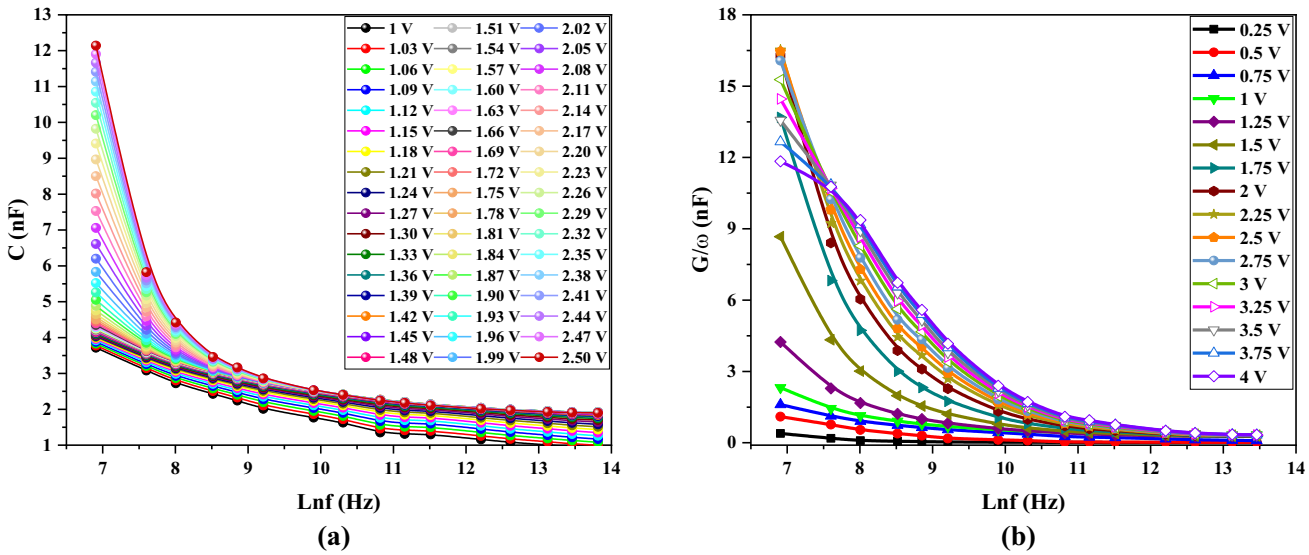

Fig. 11 Variations of (a) *C–f* and (b) *G/ω–f* profiles for the MIS-type SD.

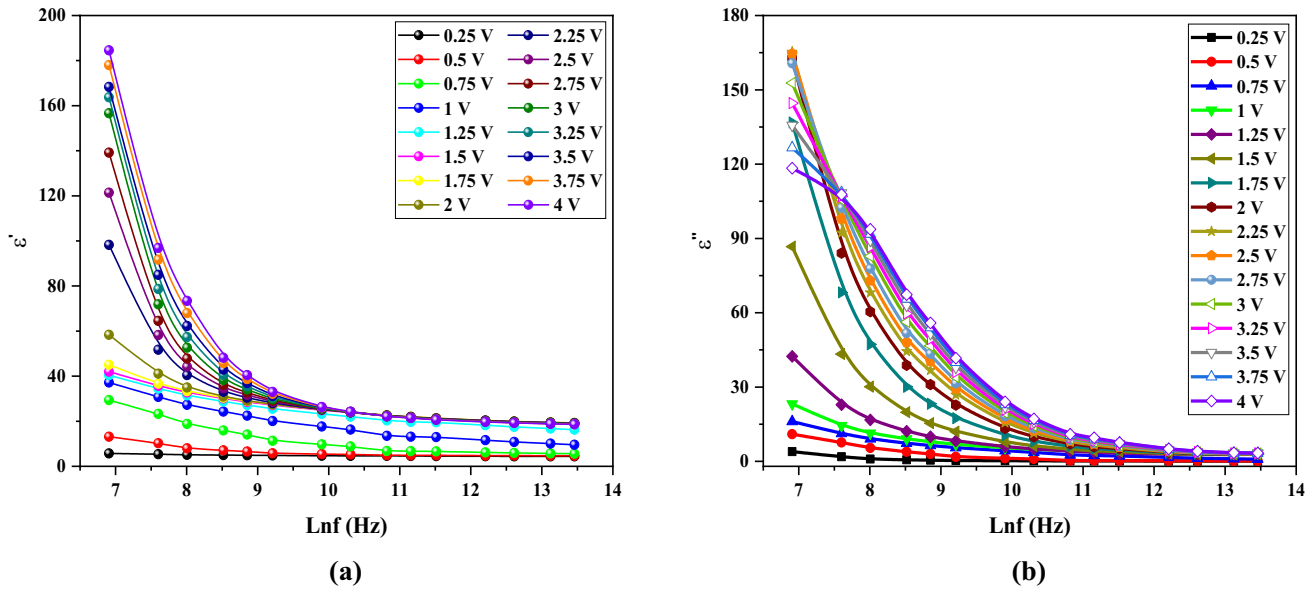

Fig. 12 Changes in (a) ε' and (b) ε'' as a function of frequency for the MIS structure.

MIS structure shows different behaviors with increasing voltage at smaller frequencies. As observed, the highest energy loss of the prepared MIS device occurs at an applied bias voltage of 2.5 V. As the frequency increases and the energy loss stabilizes at a fixed value, the impact of the bias voltage is reduced. The primary response of the MIS structure is seen at smaller frequencies because of the large resistivity of the grain boundary.[39]

In addition, the frequency dependence of tanδ for the MIS device in the bias voltage range of 0.25–4 V at room temperature is depicted in Fig. 13a. At all bias voltages, the maximum value of tanδ is found at a frequency of 5 kHz, which then shifts toward 1 kHz. After this extreme, it decreases with increasing frequency. Also, the highest and lowest values of tanδ correspond to 1.75 V and 1.25 V in the bias voltage range applied, respectively.

The frequency-dependent R_s values of the fabricated MIS structure in the bias voltage range of 0.25–4 V and frequency range of 1 kHz–1 MHz at room temperature are shown in Fig. 13b. The highest value of the R_s plots occurs at a frequency of 1 kHz, whereas the value of R_s has no change at the higher frequencies. The extremum values of R_s at 1 kHz

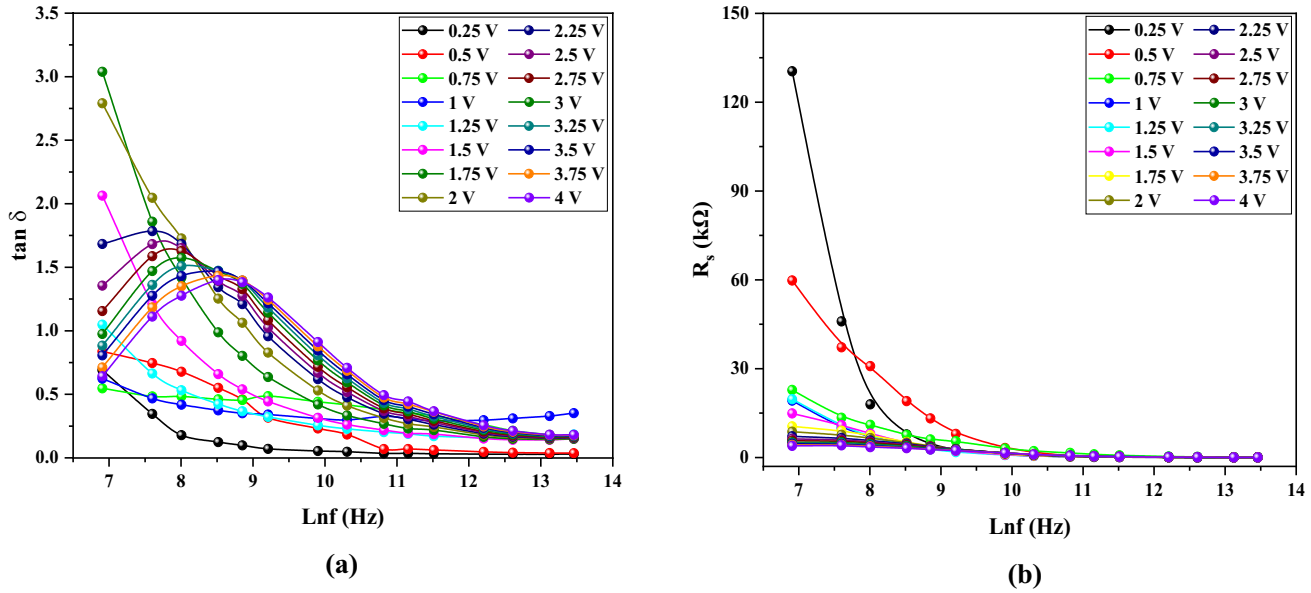

Fig. 13 Graphs of (a) tanδ–*f* and (b) R_s–*f* for the MIS-type SD.

are related to the bias voltage of 4 V and 0.25 V. It is noteworthy that the electric charges in interface traps can monitor AC signals at smaller frequencies, making a tangible contribution to the signal's value and R_s.[37,38]

The electrical conductivity is defined by the power law as[40,41]

$$\sigma = \sigma_0 + A\omega^{s_1} + B\omega^{s_2}, \tag{22}$$

where σ_0 is the DC term of electrical conductivity, ω refers to the angular frequency (2πf), and s_1 and s_2 are dimensionless frequency exponents obtained by the slope of the Ln(σ)–Ln(ω) plot. The frequency dependence of the electrical conductivity of the MIS device in the frequency range of 1 kHz–1 MHz at various bias voltages and room temperature is presented in Fig. 14. As can be observed, higher frequencies result in greater AC electrical conductivity because the interfacial polarization is reduced. Additionally, as AC conductivity increases, eddy current and energy loss both increase. Moreover, because of the DC electrical conductivity, the structures' AC electrical conductivity remains constant at lower frequencies.[41]

Similar results for electrical and dielectric properties were reported in the literature, as shown in Table III.[42–53] For example, Pakma et al.[43] examined the effects of the preparation temperature (100°C, 200°C, 300°C) on the main electrical parameters of Al/TiO_2/p-Si MIS structures and a TiO_2 interlayer prepared by the sol–gel dip-coating method. The reverse saturation current (I_0), ideality factor (n), BH (F_{B0}), and series resistance (R_s) were found to be 21 nA, 1.69, 0.519 eV, and 687.7 W for annealing at 300°C, respectively. Kınacı et al.[44] fabricated two types of SDs, Au/ZnO/TiO_2/n-Si (MIS-1) and (Ni/Au)/ZnO/TiO_2/n-Si (MIS-2). They calculated the values of n, F_{B0}, and R_s

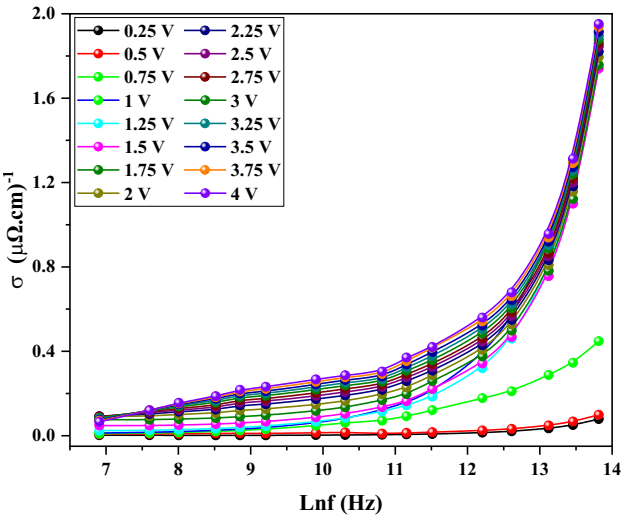

Fig. 14 Changes in σ–*f* for the MIS sample.

parameters which were equal to 1.80, 0.88 eV, and 106.2 W for MIS-1 and 1.97, 0.82 eV, and 294.8 W for MIS-2, respectively. Alialy et al.[45] fabricated a Au/TiO_2/n-4H-SiC SD and computed the values of n, F_{B0}, R_s, and R_{sh} as 5.09, 0.81 eV, 37.43 W, and 435 kW at 200 K, respectively. Kınacı et al.[46] constructed Au/TiO_2 (rutile)/n-Si (MIS) SBD and analyzed its *I–V* characteristics. They obtained the values of n, F_{B0}, and R_s as 2.59, 0.72 eV, and 71.63 W, respectively. Erdal et al.[47] prepared two SDs with the structure Al/TiO_2/n-Si and Al/Cu:TiO_2/n-Si. They calculated the values of I_0, n, F_{B0}, and R_s as 1.83×10^{-11} A, 1.93, 0.93 eV, and ~36 kW, respectively. Karabulut et al.[48] fabricated an Al/p-Si structure with a TiO_2 interlayer which was grown by

Table III A comparison of some electrical and dielectric parameters of MS structures with TiO_2 interfacial layers grown by various methods

Sample	Electrical parameters			Dielectric parameters		
	n	Φ_{B0} (eV)	R_s (W)	e'	e''	References
Au/TiO_2-surfactant/n-Si	3.81	0.80	5600	182	175	This work
Al/TiO_2/p-Si	1.69	0.52	687.7	–	–	43
Au/ZnO/TiO_2/n-Si	1.80	0.88	106.2	–	–	44
(Ni/Au)/ZnO/TiO_2/n-Si	1.97	0.82	294.8	–	–	44
Au/TiO_2/n-4H-SiC	5.09	0.81	37.43	–	–	45
Au/TiO_2 (rutile)/n-Si	2.59	0.72	71.63	–	–	46
Au/TiO_2/n-Si	1.93	0.93	–	–	–	47
Al/TiO_2/p-Si (ALD)	2.24	0.80	–	–	–	48
Au/TiO_2 (anatase)/n-Si	3.36	0.603	209.0	–	–	49
Ni/n-TiO_2/p-Si/Al	–	–	–	2	160	42
Au/TiO_2/n-Si	–	–	–	51	32	50
Au/TiO_2/n-4H-SiC	–	–	–	1.74	3.69	51
Al/TiO_2/p-Si	–	–	–	45	1000	52
(AuZn)/TiO_2/p-GaAs (110)	–	–	–	1.02	1.6 (1 MHz)	53

atomic layer deposition (ALD) with a thickness of 10 nm. They measured the *I–V* characteristics in the dark and under different illumination intensities (10 and 100 mW cm^{-2}). The values of Φ_{B0} and ideality factor (n) were found to be (0.80 eV, 1.04) in the dark, (0.70 eV, 2.24) at mW cm^{-2}, and (0.56 eV, 10.27) at 100 mW cm^{-2}. In a report by Bengi et al.[49], TiO_2 thin films were also deposited on polycrystalline *n*-type Si wafers utilizing DC magnetron sputtering, and to improve the crystal quality, they were annealed at 700°C (anatase) and 900°C (rutile). The authors found that the RR of the Au/n-Si (MS) structure with anatase-phase TiO_2 was 140, while the rutile phase was 8864. The magnitude of the leakage current for the rutile phase was 15 times lower than the anatase phase. These results show that the performance of the Au/TiO_2/n-Si structure was also improved with thermal annealing.

In a work by Kumar et al.[42], TiO_2 thin film was grown between Ni and p-Si using pulsed laser ablation to construct Ni/n-TiO_2/p-Si/Al heterojunction diodes. TiO_2 pellets were then sintered at 1000°C for 12 h and used for the deposition of thin films. The dielectric properties of the films were investigated in a wide range of applied bias voltage, temperature, and frequency. The results showed that the values of e' and e'' are strongly related to frequency, temperature, and applied bias voltage, especially at low frequencies, mainly due to the Maxwell–Wagner and space charge polarization. The e' and e'' values were found to be 2 (at 4 kHz) and 160 (at 1 MHz) at 2 V and room temperature, respectively. Büyükbaş Uluşan and Tataroğlu[50] reported the deposition of a thin film of TiO_2 onto an n-Si substrate using a radio frequency (RF) magnetron sputtering system to fabricate a Au/TiO_2/n-Si (MIS) structure.[50] The admittance (*C*/*G*–*V*) measurements were performed in the frequency range of 0.5–500 kHz at room temperature. It was observed that the dielectric constant (ε') and dielectric loss (ε'') decreased with increasing frequency, with values of 51 at 0.5 kHz and 2 at 0.5 MHz, respectively. Tanrıkulu et al.[51] fabricated an SBD with a structure of Au/TiO_2/n-4H-SiC to examine the frequency-dependent dielectric properties. The values of e', e'', and s_{ac} were found to be 1.79, 3.64, and 2.03×10^{-7} S/cm at 100 kHz and 0.34, 0.46, and 2.57×10^{-7} S/cm at 1 MHz, respectively. Gullu and Yildiz[52] studied the dielectric features of an Al/TiO_2/Si SD by calculating the values of e' and e'' from the capacitance and conductance data. They obtained values of 45 at 1 kHz and 1000 at 1 MHz, respectively, for these parameters. Şafak Asar et al.[53] reported the dielectric properties of a fabricated (AuZn)/TiO_2/p-GaAs(110) MIS structure by evaluating the e', e'', and s_{ac} values as a function of voltage and temperature, obtaining values of 1.02, 1.60, and 2.0×10^{-6} S/cm at room temperature for 1 MHz and 1.0 V, respectively.

Conclusions

In this study, an MIS-type SD with a Au/TiO_2-Brij 58/n-Si structure was fabricated on a Si wafer. The deposition process of the TiO_2-Brij 58 layer at the M/S interface was thoroughly described. By utilizing different computation methods including TE, Norde, and Cheung functions, the essential electrical parameters of the MIS device, including I_0, BH, n, R_{sh}, and R_s, were determined with the measurement of the *I–V* data at room temperature. The values of I_0, n, BH, R_{sh}, R_s, and RR for the prepared MIS device were equal to 4.59×10^{-9} A, 3.81, 0.798 eV, 524.91 MΩ, 5.60 kΩ, and 9.40×10^{4}, respectively. It was found that the TiO_2-surfactant interlayer at the interface of M/S led to a decrease in the leakage current and ideality factor and an increase in the potential barrier height and rectification ratio compared with the MS structure. Also, the presence of a TiO_2-surfactant interlayer in the MIS device decreased the N_{ss} density at the interface of M/S, originating from the

semiconductor surface passivation. It was observed that the predominant CCMs in the MS and MIS structures were the PFE and SE mechanisms, respectively, with the comparison of β values computed theoretically and experimentally. In addition, the voltage- and frequency-dependent dielectric characteristics of the fabricated MIS device were investigated by measuring the capacitance and conductance in a range of voltages (0.25–4 V) and frequencies (1 kHz–1 MHz) at room temperature. Contrary to the increase in frequency, the dielectric properties of the MIS device were increased by increasing the bias voltage applied. Three regions, i.e., inversion, depletion, and accumulation, were observed in the voltage dependence of dielectric features of the presented MIS device. These behaviors are attributed to R_s and N_{ss} at the M/S interface. The values of C and G/ω were significantly altered at lower frequencies, whereas small changes were observed at higher frequencies. Such behavior can be observed in ε', ε'', tanδ, R_s, and σ functions. This is because the electrons do not have the capability of tracking the electric field at higher frequencies.

Author Contributions All authors contributed to the study conception and design. Yashar Azizian-Kalandaragh and Halil Ibrahim Efkere: Material preparation, Data collection, Project administration; Ali Barkhordari: Writing—original draft of manuscript; Benedetta Marmiroli and Barbara Sartori: Methodology, Investigation, Writing—review and editing of the manuscript; Süleyman Özçelik: Investigation, Supervision; Golamreza Pirgholi-Givi: Data Analysis; Şemsettin Altındal: Investigation, Supervision. All authors read and approved the final manuscript.

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Data Availability The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

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References

1. S.M. Sze, Y. Li, and K.K. Ng, *Physics of semiconductor devices* (New York: John Wiley & sons, 2021).
2. H.C. Card and E.H. Rhoderick, Studies of tunnel MOS diodes I Interface effects in silicon Schottky diodes. *J. Phys. D: Appl. Phys.* 4(10), 1589 (1971).
3. R.T. Tung, The physics and chemistry of the Schottky barrier height. *Appl. Phys. Rev.* 1(1), 011304 (2014).
4. N.A. Al-Ahmadi, Metal oxide semiconductor-based Schottky diodes: a review of recent advances. *Mater. Res. Express* 7(3), 032001 (2020).
5. M.H. Al-Dharob, H.E. Lapa, A. Kökce, A.F. Özdemir, D.A. Aldemir, and Ş Altındal, The investigation of current-conduction mechanisms (CCMs) in Au/(0.07 Zn-PVA)/n-4H-SiC (MPS) Schottky diodes (SDs) by using (IVT) measurements. *Mater. Sci. Semiconduct. Process.* 85, 98–105 (2018).
6. K. Kano, *Semiconductor devices* (NJ: Prentice-Hall Englewood Clifs, 1998).
7. P. Cova, A. Singh, A. Medina, and R.A. Masut, Effect of doping on the forward current-transport mechanisms in a metal-insulator-semiconductor contact to InP: Zn grown by metal organic vapor phase epitaxy. *Solid-State Electron.* 42(4), 477–485 (1998).
8. N.R. Mathews, E.R. Morales, M.A. Cortés-Jacome, and J.T. Antonio, TiO_2 thin films-Influence of annealing temperature on structural, optical and photocatalytic properties. *Sol. Energy* 83(9), 1499–1508 (2009).
9. K.J. Han, K.S. Kang, Y. Chen, K.H. Yoo, and J. Kim, Effect of annealing temperature on the conduction mechanism for a sol-gel driven ZnO Schottky diode. *J. Phys. D Appl. Phys.* 42(12), 125110 (2009).
10. L.M. Williams and D.W. Hess, Structural properties of titanium dioxide films deposited in an rf glow discharge. *J. Vac. Sci. Technol. A: Vac. Surf. Films* 1(4), 1810–1819 (1983).
11. M. Gartner, C. Parlog, and P. Osiceanu, Spectroellipsometric characterization of lanthanide-doped TiO_2 films obtained via the sol-gel technique. *Thin Solid Films* 234(1–2), 561–565 (1993).
12. H. Tang, K. Prasad, R. Sanjines, P.E. Schmid, and F. Levy, Electrical and optical properties of TiO_2 anatase thin films. *J. Appl. Phys.* 75(4), 2042–2047 (1994).
13. M.C. Fuertes, F.J. López-Alcaraz, M.C. Marchi, H.E. Troiani, V. Luca, H. Míguez, and G.D. Soler-Illia, Photonic crystals from ordered mesoporous thin-film functional building blocks. *Adv. Func. Mater.* 17(8), 1247–1254 (2007).
14. A. Barkhordari, H.R. Mashayekhi, P. Amiri, Ş Altındal, and Y. Azizian-Kalandaragh, Role of graphene nanoparticles on the electrophysical processes in PVP and PVP: $ZnTiO_3$ polymer layers at Schottky diode (SD). *Semicond. Sci. Technol.* 38(7), 075002 (2023).
15. V.R. Reddy and C.V. Prasad, Surface chemical states, electrical and carrier transport properties of Au/ZrO_2/n-GaN MIS junction with a high-k ZrO_2 as an insulating layer. *Mater. Sci. Eng. B* 231, 74–80 (2018).
16. M. Sharma and S.K. Tripathi, Frequency and voltage dependence of admittance characteristics of Al/Al_2O_3/PVA: n-ZnSe Schottky barrier diodes. *Mater. Sci. Semicond. Process.* 41, 155–161 (2016).
17. A. Barkhordari, Ş Altındal, G. Pirgholi-Givi, H. Mashayekhi, S. Özçelik, and Y. Azizian-Kalandaragh, The influence of PVC and (PVC: SnS) interfacial polymer layers on the electric and dielectric properties of Au/n-Si structure. *Silicon* 15(2), 855–865 (2023).
18. O. Çiçek, H.U. Tecimer, S.O. Tan, H. Tecimer, Ş Altındal, and I. Uslu, Evaluation of electrical and photovoltaic behaviours as comparative of Au/n-GaAs (MS) diodes with and without pure and graphene (Gr)-doped polyvinyl alcohol (PVA) interfacial layer under dark and illuminated conditions. *Compos. B Eng.* 98, 260–268 (2016).
19. S. Fuentes, R.A. Zárate, E. Chávez, P. Munoz, M. Ayala, R. Espinoza-González, and P. Leyton, Synthesis and characterization of $BaTiO_3$ nanoparticles in oxygen atmosphere. *J. Alloy. Compd.* 505(2), 568–572 (2010).
20. S. Parhoodeh and M. Kowsari, Synthesis, characterization and study of band gap variations of vanadium doped indium oxide nanoparticles. *Physica B* 498, 27–32 (2016).
21. P. Thiruramanathan, A. Marikani, D. Madhavan, S. Bharadwaj, and A.M. Awasthi, Influence of calcination temperature on sol-gel synthesized single-phase bismuth titanate for high dielectric capacitor applications. *Int. J. Mater. Res.* 107(5), 484–492 (2016).
22. A. Tataroğlu, A.A. Hendi, R.H. Alorainy, and F. Yakuphanŏlu, A new aluminum iron oxide Schottky photodiode designed via sol-gel coating method. *Chin. Phys. B* 23(5), 057504 (2014).

23. A. Buyukbas-Uluşan, S. Altındal Yerişkin, A. Tataroğlu, M. Balbaşı, and Y.A. Kalandaragh, Electrical and impedance properties of MPS structure based on (Cu_2O–CuO–PVA) interfacial layer. *J. Mater. Sci. Mater. Electron.* 29, 8234–8243 (2018).
24. H. Schroeder, Poole-Frenkel-effect as dominating current mechanism in thin oxide films-An illusion? *J. Appl. Phys.* 117(21), 215103 (2015).
25. E. Marıl, A. Kaya, S. Koçyiğit, and Ş Altındal, On the analysis of the leakage current in Au/$Ca_3Co_4Ga_{0.001}$Ox/n-Si structure in the temperature range of 80–340 K. *Mater. Sci. Semiconduct. Process.* 31, 256–261 (2015).
26. B.L. Sharma, *Physics of Schottky barrier junctions metal-semiconductor contacts Schottky barrier junctions and their applications* (New York and London: Plenum Press, 1984).
27. A. Barkhordari, S. Özçelik, G. Pirgholi-Givi, H.R. Mashayekhi, Ş Altındal, and Y. Azizian-Kalandaragh, Dielectric properties of PVP: $BaTiO_3$ interlayer in the Al/PVP: $BaTiO_3$/P-Si structure. *Silicon* 14(10), 5437–5443 (2022).
28. H. Uslu, Ş Altındal, T. Tunç, İ Uslu, and T.S. Mammadov, The illumination intensity and applied bias voltage on dielectric properties of au/polyvinyl alcohol (Co, Zn-doped)/n-Si Schottky barrier diodes. *J. Appl. Polym. Sci.* 120(1), 322–328 (2011).
29. O. Bidault, P. Goux, M. Kchikech, M. Belkaoumi, and M. Maglione, Space-charge relaxation in perovskites. *Phys. Rev. B* 49(12), 7868 (1994).
30. Z. Tekeli, M. Gökçen, Ş Altındal, S. Özçelik, and E. Özbay, On the profile of frequency dependent dielectric properties of (Ni/Au)/GaN/$Al_{0.3}Ga_{0.7}$N heterostructures. *Microelectron. Reliabil.* 51(3), 581–586 (2011).
31. I.M. Afandiyeva, İ Dökme, Ş Altındal, M.M. Bülbül, and A.D. Tataroğlu, Frequency and voltage effects on the dielectric properties and electrical conductivity of Al–TiW–Pd2Si/n-Si structures. *Microelectron. Eng.* 85(2), 247–252 (2008).
32. C.P. Smyth, *Dielectric Behaviour and Structure* (New York: McGraw-Hill, 1955).
33. P. Pissis and A. Kyritsis, Electrical conductivity studies in hydrogels. *Solid State Ionics* 97(1–4), 105–113 (1997).
34. M. Popescu and I. Bunget, *Physics of solid dielectrics* (Amsterdam: Elsevier, 1984).
35. A. Chelkowski, *Dielectric Physics* (Amsterdam: Elsevier, 1980).
36. H. Tecimer, H. Uslu, Z.A. Alahmed, F. Yakuphanoğlu, and Ş Altındal, On the frequency and voltage dependence of admittance characteristics of Al/PTCDA/P-Si (MPS) type Schottky barrier diodes (SBDs). *Compos. B Eng.* 57, 25–30 (2014).
37. D.K. Schroder, *Semiconductor material and device characterization* (New York: John Wiley & Sons, 2015).
38. D. Seghier and H.P. Gislason, Electrical characterization of Mg-related energy levels and the compensation mechanism in GaN: Mg. *J. Appl. Phys.* 88(11), 6483–6487 (2000).
39. F.B. Abdallah, A. Benali, M. Triki, E. Dhahri, M.P. Graca, and M.A. Valente, Effect of annealing temperature on structural, morphology and dielectric properties of $La_{0.75}Ba_{0.25}FeO_3$ perovskite. *Superlatt. Microstruct.* 117, 260–270 (2018).
40. A. Barkhordari, H. Mashayekhi, P. Amiri, Ş Altındal, and Y. Azizian-Kalandaragh, On the investigation of frequency-dependent dielectric features in Schottky barrier diodes (SBDs) with polymer interfacial layer doped by graphene and $ZnTiO_3$ nanostructures. *Appl. Phys. A* 129(4), 249 (2023).
41. G. Bator, Ac and dc conductivity around the ferroelectric phase transition in $(CH_3NH_3)_3Bi_2Br_9$ (MABB) crystal. *Ferroelectrics* 200(1), 287–295 (1997).
42. A. Kumar and K. Sharma, Investigation of dielectric properties of Ni/N-TiO_2/P-Si/Al heterojunction in wide range of temperature and voltage. *Int. J. Eng. Trans. A* 35(4), 698–705 (2022).
43. O. Pakma, N. Serin, T. Serin, and Ş Altındal, The effects of preparation temperature on the main electrical parameters of Al/TiO_2/p-Si (MIS) structures by using sol–gel method. *J. Sol-Gel Sci. Technol.* 50(1), 28–34 (2009).
44. B. Kinaci, T. Asar, S.Ş Çetin, Y. Özen, and K. Kizilkaya, Electrical characterization of Au/ZnO/TiO_2/n-Si and (Ni/Au)/ZnO/TiO_2/n-Si Schottky diodes by using current-voltage measurements. *J. Optoelectron. Adv. Mater.* 14(11), 959 (2012).
45. S. Alialy, Ş Altındal, E.E. Tanrıkulu, and D.E. Yıldız, Analysis of temperature dependent current-conduction mechanisms in Au/TiO_2/n-4H-SiC (metal/insulator/semiconductor) type Schottky barrier diodes. *J. Appl. Phys.* 116(8), 083709 (2014).
46. B. Kınacı, S.Ş Çetin, A. Bengi, and S. Özçelik, The temperature dependent analysis of Au/TiO_2 (rutile)/n-Si (MIS) SBDs using current–voltage–temperature (I–V–T) characteristics. *Mater. Sci. Semicond. Process.* 15(5), 531–535 (2012).
47. M.O. Erdal, A. Kocyigit, and M. Yıldırım, Temperature dependent current-voltage characteristics of Al/TiO_2/n-Si and Al/Cu:TiO_2/n-Si devices. *Mater. Sci. Semicond. Process.* 103, 104620 (2019).
48. A. Karabulut, İ Orak, and A. Türüt, The photovoltaic impact of atomic layer deposited TiO_2 interfacial layer on Si-based photodiodes. *Solid-State Electron.* 144, 39–48 (2018).
49. A. Bengi, U.M. Aydemir, Ş Altındal, Y.U. Özen, and S. Özçelik, A comparative study on the electrical characteristics of Au/n-Si structures with anatase and rutile phase TiO_2 interfacial insulator layer. *J. Alloy. Compd.* 505(2), 628–633 (2010).
50. A.B. Uluşan and A.D. Tataroğlu, Frequency-dependent dielectric parameters of Au/TiO_2/n-Si (MIS) structure. *Silicon* 10, 2071–2077 (2018).
51. E.E. Tanrıkulu, D.E. Yıldız, A. Günen, and Ş Altındal, Frequency and voltage dependence of electric and dielectric properties of Au/TiO_2/n-4H-SiC (metal-insulator-semiconductor) type Schottky barrier diodes. *Phys. Scr.* 90(9), 095801 (2015).
52. H.H. Gullu and D.E. Yildiz, Capacitance, conductance, and dielectric characteristics of Al/TiO_2/Si diode. *J. Mater. Sci. Mater. Electron.* 32, 13549–13567 (2021).
53. Y. Şafak Asar, T. Asar, Ş Altındal, and S. Özçelik, Dielectric spectroscopy studies and ac electrical conductivity on (AuZn)/TiO_2/p-GaAs (110) MIS structures. *Phil. Mag.* 95(26), 2885–2898 (2015).