A Delay-Locked-Loop with a Quasi-Linear Modified Differential Delay Element

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Abstract— A Delay-Locked-Loop with a quasi-linear modified differential delay element is presented. By employing body feed technique in the bias circuit of delay cell in the Multi-Controlled-Delay-Line, applicable range for the controlled signal has been widen to under-threshold voltages, also the nonlinearity of the conventional current starved delay element the has been suppress by bias circuit. Moreover, improving the noise performance is achieved by taking advantage of the differential structure in the delay cell. The designed circuit has been simulated in ADS software, using TSMC-CM018RF Process with a 1.8V supply voltage. The operating frequency range of the proposed DLL is from 280 MHz to 820 MHz. The maximum and minimum rms jitters are 18 and 4.2 ps, at 280MHz and 820MHz respectively. The maximum power dissipation of designed circuit at 820 MHz is 4.13mW.

Index Terms— Delay element, body feed technique, delay locked loop, bias circuit.

1 Introduction

In recent years, DLL has attracted great attention for integrated circuits, such as timing recovery [1], BIST circuit [2], and frequency multiplier [3]. Usually, the input signal to generate the output signal goes throw the delay line under the control of feedback circuit, so its characteristics significantly affect the whole performance of the loop. For example, in analog DLLs the delay range of the Voltage- Controlled – Delay -Line (VCDL) will directly limit the operating range of the circuit [4]. The controlled voltage is generally bounded by the supply voltage and the threshold voltage of the transistors; When the VC is nearby transistor threshold voltage, the delay is very sensitive to variations in the VC and noise [5]. Moreover, a serious problem with conventional VCDL structure is that the variation of output propagation delay is not linearly related to the control voltage (VC)[6], which greatly reduces the performance of the VCDL at low frequencies.

In the proposed DLL to improve the linearity of the Delay-Line and allow rail-to-rail operation for the delay control voltage, a differential current starved delay cell with proper bias circuit is proposed. The rest of this paper is organized as follows: Section 2 explains the architecture of the proposed MMDLL and detail circuits within delay line are discussed in section 3. The simulation results are shown in Section 4, and conclusions are given in Section 5.

2 Proposed DLL Circuit

The simple loop characteristics belie many subtleties in DLL design. Increasing demand for high frequency operation and low jitter performance propels DLL design to mixed-signal technology. In order to achieve improved jitter performance, the DLL should have a delay stage with low supply and substrate noise sensitivity and to realize the high-frequency DLL, the bandwidth requirement of the delay cells in the Delay-Line should be considered.

In this work, to enhance the operating range a multi-period-locked technique [7] with a selectable locked period is adopted. Simplified building block of the proposed DLL is outlined in the Figure 1, consists of a Multi-Controlled-Delay-Line (MCDL) with five delay stages and two dummy cells, a start-controlled PFD (SCPFD)[8], a CP, a loop filter (LF), two divide-by-2 circuits, two de-multiplexers, and five 2-1 multiplexers. The multiplexers are inserted in the outputs of the delay cells to output the clocks sequentially and match the loads. The de-multiplexers are used to select or bypass the dividers to enlarge the operation range of DLL in high frequencies. In this way, frequency range is divided into high frequency and low frequency regions. When the signal HF is low, the DLL acts as a conventional one, and in the case of HF=1, frequency range is increased by a factor of two, explained later, and the DLL acts in high frequency band. The detailed operation of DLL will now be explained when HF is high.

In the beginning, the start signal is set to logic 0; the DLL is disabled; the SCPFD is in the reset mode; the UP and DN signals are low and no current flows the charge pump through the loop capacitor. Also, the VC is set to VDD, and the delay from the MCDL is forced initially to its minimum value. When the start signal becomes high and a reference clock progresses through the MCDL, the input clock and the output clock of the delay line are divided by two. The divider outputs, REF and FED, are connected to the SCPFD. Although, the input and output signals of the delay-line are in the same frequency with the input signal, when this MDLL is locked, the total delay of the MCDL is twice the period of input clock, because the frequency of REF and FED are 2x lower than the input signal. In this way, the proposed MMDLL can be locked at the signal by the period of 2x lower that minimum delay of its MCDL, which means that, the useful frequency range of the proposed MDLL is increased by 2 times. However, the size of MCDL is doubled too [7], which may consume a lot of power and

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degrades the output jitter performance. To save the MCDL and achieve the wide-range MMDLL, the divider circuits are used only when the MMDLL works within high frequency band, and conventional method is adopted when the DLL works within low frequency band. Moreover, since the input signals of SCPFD are FED and REF, there is no probability for phase ambiguity. In lock condition output phases of the five delay cells will be:

$$\frac{2}{5}T_{in}, \frac{4}{5}T_{in}, \frac{1}{5}T_{in}, \frac{3}{5}T_{in}, \frac{5}{5}T_{in} \quad (1)$$

Where, Tin denotes the period of input clock. In other words it is equivalent to (2π). As can be seen, the phase sequence is not monotonic in this condition. To have the monotonic phase outputs, the outputs of the delay cells can be appropriately routed by multiplexers. For example, the input pin of the MUX for CK1, active when HF=0, is connected to output of the first delay cell and its other input, active when HF=1, is connected to the third delay cell.

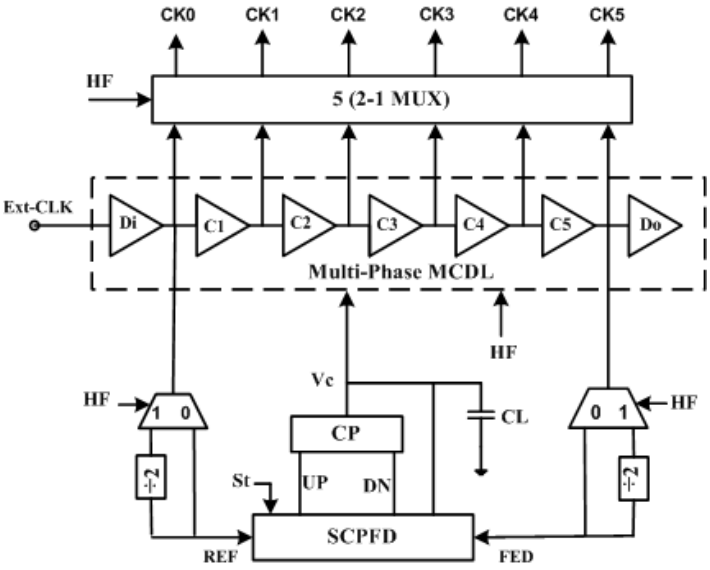


Fig 1. The building block of proposed DLL

3 THE MCDL

First step in DL design is selecting the basic delay cell. In this work the current-starved inverter is chosen due to full swing capability, both rise and fall time tunability and fast-slewing. Conventional Current-starved-delay-elements (CSDEs) [9] have two main problems. First is its sensitivity to power supply and substrate noise, especially noticeable in the environment of mixed-signal ICs. Second is that the variation of output propagation delay is not linearly related to the control voltage. In the proposed delay cell at [10], two single ended current starved inverters are utilized in a differential structure. A differential architecture will have better power-supply rejection ratio (PSRR) and a superior noise performance compared to single-ended ring architecture. Each delay stage produces a pair of large signal differential waveforms that drive a similar delay stage within the delay line path, whereas unlike conventional differential structures it consumes negligible DC power. Each branch of the delay cell is implemented as a two-stage inverter; delay value is adjusted by the charge/discharge current that flows through the first inverter. Moreover, cross-coupled inverters are inserted at the output nodes to reduce the clock skew between the 0 and 180 clocks. Main problem with this structure is that each cell has a body biased transistor. Separating a body terminal for NMOS transistor in TSMC CMOS technology consumes a lot of area. Moreover, this cell is designed at supply voltage of 1.2V and maximum frequency of the cell is 500MHz. To increase the frequency range of delay cell, 1.8V for supply voltage is selected; the cell has not linear behavior at this supply voltage.

In this work, body bias transistor is transferred from delay cell to bias circuit to save the die area; thus only one NMOS transistor controlled by body terminal exists in whole of delay line. As shown in Figure 2, all the starved transistors, MN1/MP1 and MN2/MP2, are controlled by gate terminal. An auxiliary current path, established by PMOS and NMOS transistors, MN3 and MP3, helps to reduction of the cell delay to decrease the delay of the cell when the DLL acts at high frequency range and the HF signal is in logic 1. Figure3 illustrates overall transfer function of a conventional CSDE. As shown in the figure, this delay cell can span from minimum buffer delay to infinite. By careful attention to the curve, three different parts of 1, 2 and 3 can be recognized. Part 1 called dead-band region [4]. When the VC is smaller than the threshold, the device enters the sub-threshold region and the DL cannot provide the delay. In other words dead-band issue decreases controllable voltage region of the delay line, resulting in the VCDL operating in a narrow band of control voltage. In part 2, the VC is near the threshold voltage. As operating in this region, the delay is very sensitive to variations in the VC and noise at low frequencies. The slope of curve decreases in the part3. Extremely, low slope loses useful controllable voltage region. In this work, nonlinear behavior over narrow band of the control voltage is corrected by applying variable bias generator. The suggested circuit, shown in Figure 4, balances the gain of the delay line in whole range of control voltage by generating proper control current for starved transistors (MN1/MP1, MN2/ MP2 in Figure 2) of delay cell from output voltage of loop filter (VC). As can be seen in the Figure 4, the circuit is composed of three different circuits and creates the currents I1, I2, and I3, respectively activated in regions 1, 2, and 3, illustrated in Figure 3. To overcome the dead-zone issue and get required current in region 1, body bias technique is used [11].

When the control signal is lower than transistor threshold voltage, the transistors MN4 and MN8 turn off, so the currents I2 and I3 are zero and due to fixed bias at the gate of MN3, it is on and the current of the bias circuit is solely provided by I1. The current I1 is current of body controlled transistor, MN3. Control voltage of MN3 is created by MN1/MP1 and MN2/MP2, proportional to VC. In other words the sub-threshold current of MN1 provides a forward body bias for MN3, which effectively reduces its threshold voltage. Thus, the bias current increases monotonically with

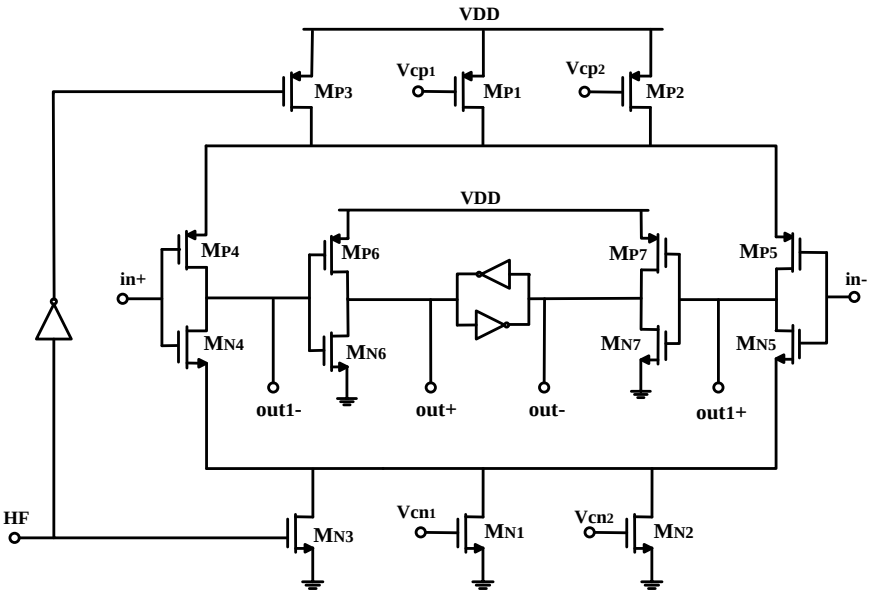


Fig. 2. The proposed delay cell

the control voltage. When the control signal reaches the threshold voltage, body-source junction of MN3 starts to be forward bias, so the voltage of body terminal and I1 will be fixed and act as a constant current source in bias circuit, which help to reduce the gain of the MCDL in the region 2 and improve the linearity. When the VC locates in part 2, transistor MN4 will turn on and adjust the current of bias circuit. To reduce the gain of delay line in region 2, W/L ratio of MN4 should be small (3/12). Addition of I1 and I2 is mirrored by MP3 and MP4 and made the control voltage in MN5. In high values of VC, I3 is the effective one. Because of diode-connected transistor MN7, the MN8 will be turn on at about twice the threshold voltage. Since increasing the gain of delay line is desired in region 3, size of MN8 is chosen to be large (12/3).

In a real implementation, gates and drain connection nodes in current mirrors introduce poles in the VCDL transfer function. Thus, there is a design trade-off with size of the transistors of current mirror, and care must be taken so they are at high frequencies not to disturb dynamic behavior of DLL. For this purpose, the size of these transistors must be chosen as small as possible. On the other hand, the small ratio of W/L decreases compliance voltage of current mirror. Therefore, a proper trade-off has to be made in the size of current mirrors. It is worth noting that almost all PMOS transistors have an aspect ratio three times larger to account for their lower mobility. In this way, the bias circuit controls the current available to charge or discharge the load capacitance of the first inverter in the whole range of control voltage from 0.2V to 1.6V. As mentioned before the purpose of bias circuit is making a linear transfer curve for delay cell.

Since delay is inversely proportional with bias current, if the current (I) relates to voltage (V) by the function Y=1/X, the final delay will behavior linearly with voltage. By shifting the curve Y=1/X to right on x-axis, the curve Y=A/(B-X) will be achieved, Where, A and B are constant number; in summary if the relation between I and V in a delay line can be expressed as I=A/(B-V)

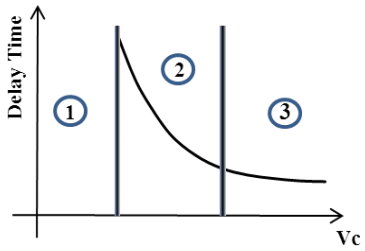


Fig. 3. Transfer function of conventional CSDE.

that delay line will behavior linearly. Figure 5(a) shows bias current versus control voltage, interpolated by the desired function with A = 26.67 and B = 1.8. Total delay curve, interpolated by a linear function, is also shown in Figure 5(b). As can be seen, the slope of conventional CSDE is balanced and a good linearity in a wide dynamic range for the delay control signal is achieved. By comparing two curves in Figure 5(a) and Figure 5(b), it can be deduced that in a specified value of VC by increasing the difference of the bias current and desired function in Figure 5(a), distinction of the delay from the linear function will be enlarged at Figure 5(b). As can be seen, in VC=1.6, there is a maximum difference between the real and interpolated value in both Figures. The utilized multiphase MCDL (Figure 6.) is similar to the one proposed in [10] . It composed of five delay cell units to generate the five multiphase output. In other words, each delay element produces on-chip five-phase clocks that are 72 degrees apart in one period; phase blenders can be used to further increase the phase resolution of the DL. Additional dummy delay cells are used to equalize the environment of all the cells and therefore improve delay matching. Two inverters, added to the output of each delay stage, cancel the loading effect of the sub-blocks, connected to the output of delay stages.

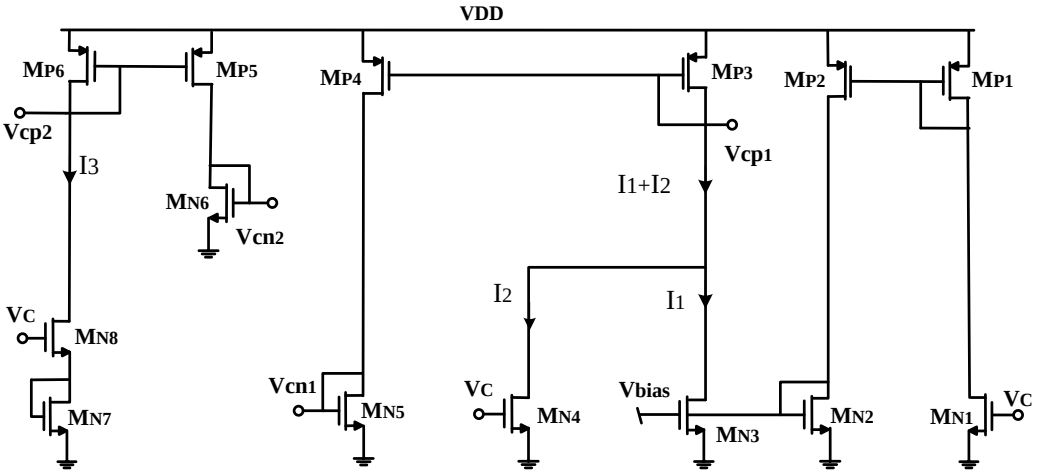
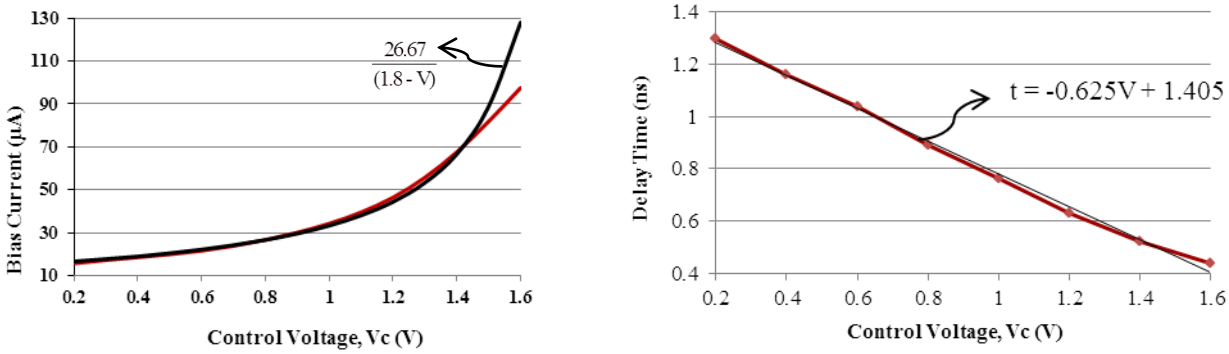


Fig. 4. Variable bias voltage generator.



(a) (b)

Fig. 5. (a) DC curve of bias circuit. (b) Output delay versus control voltage.

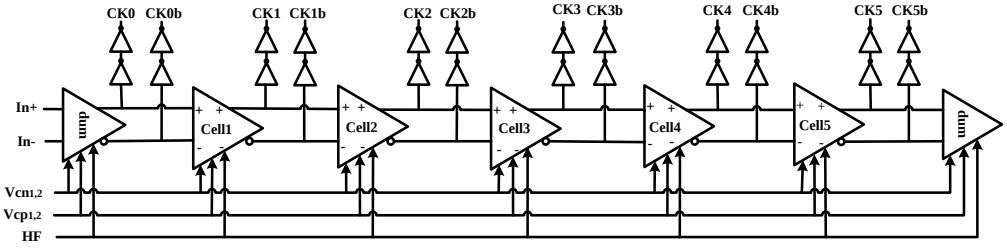


Fig. 6. The proposed multiphase delay line.

4 Simulation Results

The proposed circuit has been designed at transistor level and simulated by ADS, using 0.18um CMOS process. First, locking process at normal condition (TT technology, 25˚C and 1.8V supply voltage) has been illustrated. Input and output signals during the lock process have been illustrated in Figure 7. Then some periods of multiphase outputs in lock condition at minimum and maximum frequencies of loop are shown in Figures 8 and 9. Minimum and maximum frequencies that the loop can lock in normal conditions are 170MHz and 1100MHz respectively. Moreover, to evaluate the DLL performance at process, supply voltage and temperature (PVT) variations simulations have been repeated at fast condition (FF technology, -40˚C, 1.9V supply voltage) and slow condition (SS technology, 85˚C, 1.7V supply voltage). Summary of all simulation results have been shown in table 1. As can be seen the jitter and power consumption are suitable for all conditions, but considering all conditions the useful lock range is limited to be from 280MHz to 820MHz. In other words, fast condition reduces lock range of the DLL at low frequencies, and slow condition at high frequencies limits the operation range of the loop. Figure 10 shows signals of input and output nodes at boundary frequencies of 820MHz of fast corner and 280MHz of slow corner. It is obvious that the loop has proper behavior at 820MHz in fast and typical corners. Also it can lock doubtlessly at 280MHz in slow and typical corners.

In order to simulate the noise performance of the proposed DLL, transient noise simulation, available in the ADS, is used. Noise bandwidth is selected 15GHz. Also, for simulating power supply and substrate noise we have added a noise with amplitude of 10% supply voltage with the frequency of the output signal and three harmonics of it for the simulated supply sensitivity. The maximum power dissipation at 820 MHz is 4.13 mW. Due to the fact that the power consumption of DLL is dominated by its delay line, and in this work the proposed delay cell consumes negligible power, power dissipation of the total loop is low. In the table 2 the performance of the proposed circuit is compared with some of previously reported. It can be seen that frequency range of proposed structure is extended whereas power consumption and jitter are maintained at a good range.

Conclusions

This paper proposes a DLL with wide-range linear delay element CP. By proper modification into previously reported differential current starved structure and employing a new bias generator circuit, in terms of control voltage the proposed delay line has a linear delay transfer function in the whole range of regulation. Also, the effect of the power supply/substrate noise is eliminated by utilizing a differential architecture. Improvement is achieved at a cost of small hardware overhead in respect to the standard solution. The circuit design and ADS simulation are carried out by TSMC 0.18 um CMOS process. Simulation results show that the frequency range of the suggested MDLL is from 280 to 820 MHz. Maximum, and minimum rms jitters are 18 and 4.1ps, respectively, and the maximum power dissipation at 820 MHz is 4.13mW, so it is well suited for low-power applications.

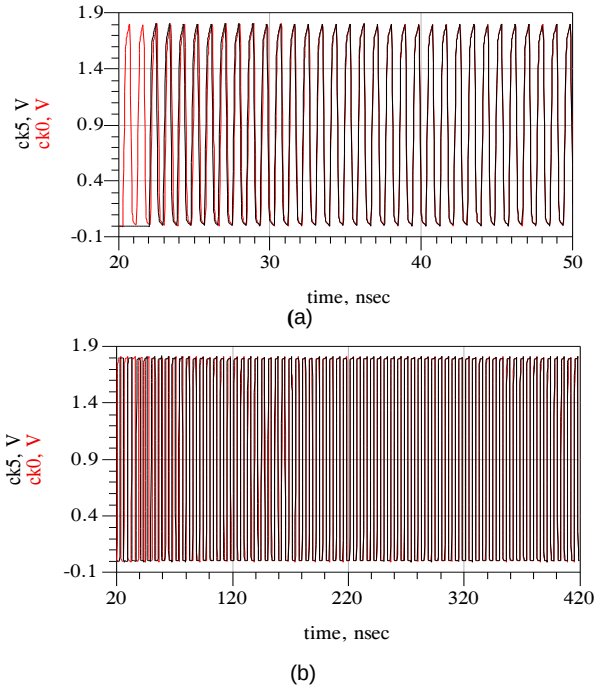


Figure 7. DLL locking process at 1100 MHz (a) 1100MHz (b)170MHz

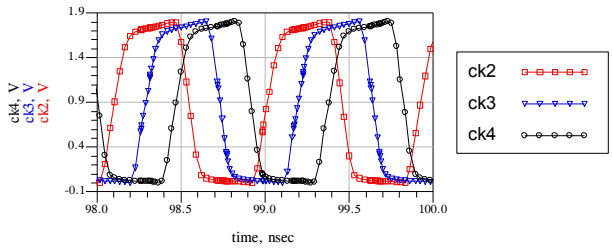


Fig. 8. Multiphase outputs at 1100MHz.

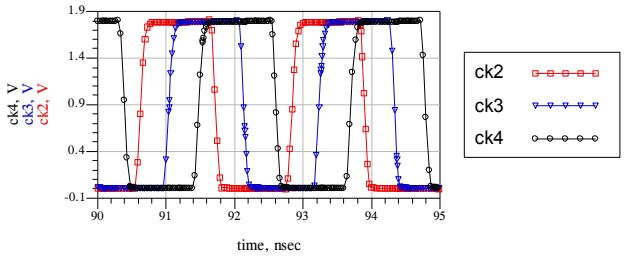


Fig. 9. Multiphase outputs at 170MHz.

TABLE 1
Summary of all simulation results.

Corners	VDD (V)	T (°C)	Jit.@500MHz (ps)	Fmin (MHz)	Fmax (MHz)	Power@ 500MHz (mW)
Typical (TT)	1.8	85	10	170	1100	2.98
Slow (SS)	1.6	25	17.7	110	820	2.93
Fast (FF)	2	-40	6.8	280	1220	3.04

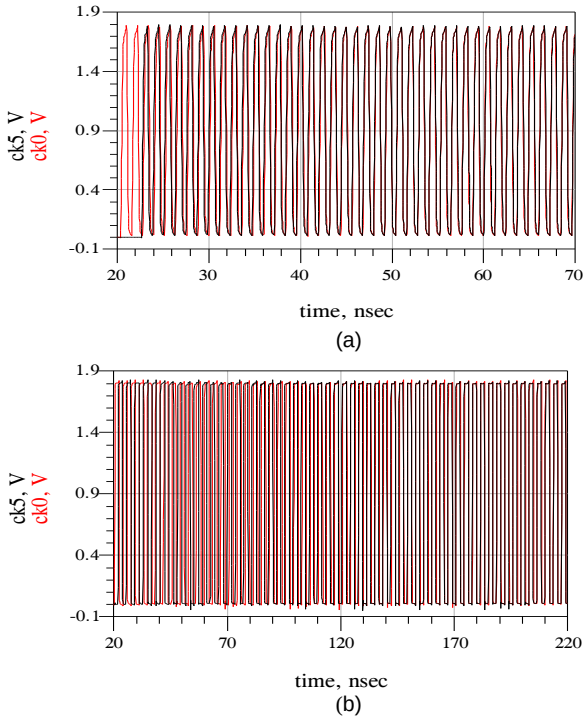


Fig. 10 DLL locking process at (a) 820 MHz at slow corner (b) 280MHz at fast corner

TABLE 2
COMPARISON WITH OTHER DLLS

Power dissipation	RMS jitter	Operation Range	Supply Voltage	Process	Reference
4.13mW @ 820MHz	4.2psec @ 820MHz	280MHz - 820MHz	1.8 V	0.18µm	This Work
21mW @ 420MHz	1.2psec @ 420MHz	120MHz - 420MHz	1.8 V	0.18µm	*[2]
4.5mW @ 400MHz	20psec @ 200MHz	200MHz - 400MHz	1.8 V	0.18µm	*[5]
1.8mW @ 120MHz	5.9psec @ 120MHz	30MHz - 120MHz	1.8 V	0.13µm	**[12]
31.5mW @ 300MHz	3.22 psec@ 300MHz	200MHz -400MHz	1.8 V	0.18µm	**[13]

*Results are from simulation
** Results are from measurement

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